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A graph-theoretic framework for analyzing the speeds and efficiencies of battery pack equalization circuits

Yang Chen[a,b], Xiaofang Liu[a], Hosam K. Fathy[b], Jiming Zou[a], Shiyan Yang[a,*]

[a] School of Electrical Engineering and Automation, Harbin Institute of Technology, 92 West Dazhi Street, Harbin 150001, China
[b] Department of Mechanical and Nuclear Engineering, Pennsylvania State University, University Park, PA 16802, United States

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ABSTRACT

This article presents a framework for analyzing the speeds and efficiencies of different battery pack balancing circuits. The article is motivated by the growing need for fast and efficient charge balancing in lithium-ion battery packs. There is an excellent literature on the design of different balancing circuits, including both single- and multi-layer active and passive topologies. However, this literature lacks a formal framework for representing different balancing circuits in a compact manner conducive to quantitative analysis. We address this challenge by representing the balancing pathways between different cells in a battery pack using a directed graph. This makes it possible to systematically analyze: (i) the "completeness" of a balancing circuit (the ability to address the imbalance between any two cells directly, even if they are not adjacent); (ii) the shortest path for balancing any two given cells; and (iii) the average efficiency of a balancing circuit for a statistical distribution of imbalance scenarios. The proposed framework is flexible: it can represent both single-layer and multi-layer balancing circuits, including circuits with multiple distinct types of converters. We demonstrate the capabilities of this framework through an example study involving the comparison of multiple balancing circuits for a 16-cell lithium-ion battery pack.

1. Introduction

This article presents a formal framework for analyzing the equalization speeds and efficiencies of different battery pack balancing topologies. The article focuses specifically on lithium-ion battery packs, which are known to provide an excellent combination of high energy density and long cycle life [1]. Since the terminal voltage of a single lithium-ion battery is very low, these batteries are usually assembled into long series strings to meet load voltage requirements. Discrepancies in manufacturing, environmental conditions, and usage can trigger substantial heterogeneities among the cells in a given series string. This may have an adverse effect on cell efficiencies, capacities, and lifetimes, which in turn can increase the risk of catastrophic events such as thermal runaway during repeated charge/discharge operation [2–4]. Equalization circuits are therefore necessary for series-connected battery strings to prevent the above problems and increase the overall lifetime of the strings [5,6].

The literature already presents many battery pack equalization circuit designs. One can classify these designs into two categories [7,8]: *passive* equalization methods and *active* equalization methods. Passive methods dissipate the excess energy of the highest-voltage battery cell by discharging this cell through a resistor. This is done repeatedly until all cells reach the same charge level [9,10]. One advantage of passive balancing is its simplicity, but this advantage comes at the cost of inefficiency and excessive heat generation. Because of these disadvantages, the application of passive balancing in high-power systems is limited. In contrast, active balancing methods typically use external circuits to transfer charge and energy among different battery cells in order to balance their voltages or states of charge (SOCs). This increases balancing circuit complexity, but has the potential to provide significant advantages in balancing speed and efficiency.

There are four different types of active balancing circuits, namely, *cell bypass*, *cell-to-cell*, *cell-to-pack*, *pack-to-cell*, and *mixed* architectures. We examine each of these categories briefly below:

1.1. Cell bypass architectures

Cell bypass balancing methods can be classified into: the *complete shunting method*, *shunt resistor*-based method, and *shunt transistor*-based methods.

The *shunt transistor* equalization method is examined extensively in references such as [11–14]. According to these references, the

* Corresponding author at: No. 92 West Dazhi Street, Nangang District, Harbin Institute of Technology, Harbin 150001, China.
E-mail addresses: 13B906036@hit.edu.cn (Y. Chen), syyang@hit.edu.cn (S. Yang).

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equalization process starts when individual cells reach their maximum/minimum reference voltages. Through a feedback network based on transistors and operational amplifiers working as comparators versus the reference voltages, the different cells are bypassed, keeping the cells' voltages at approximately the maximum reference cell voltage. This equalization approach does not exploit model-based control, and must start at the end of the charging process, with a low battery current. As a result, the equalization time, and therefore the full charging time, can be very long.

Complete shunting [15–18] and *shunt resistor* [13,14,19–21] balancing methods can achieve equalization through the constant switching between normal operation and bypassed operation for a given cell. However, this can introduce voltage fluctuations that make control more laborious, and in addition it makes difficult for battery management systems to estimate the true state of the batteries in a given pack. Secondly, when cell voltages approach their maximum values, voltage fluctuations can exceed this maximum value, and so this method is not convenient for safe control. As a result, existing control strategies are only performed at the end of the charging process, with low battery current.

1.2. Cell-to-cell architectures

As the name implies, cell-to-cell architectures address imbalance in a battery pack by transferring energy directly between pairs of unbalanced cells. One can classify these architectures into *adjacent* and *direct* architectures. In an adjacent cell-to-cell balancing topology, neighboring cells exchange energy directly with each other. One way to achieve this is to connect adjacent cells using bi-directional Buck-Boost converters [22,23]. The sizes of these converters can be greatly reduced when a high switching frequency is employed, and it is easy to modulate the converters. Improvements on the simple Buck-Boost and Cuk architecture exist in the literature [24–31], but all adjacent cell-to-cell balancing architectures suffer from one disadvantage: the average path needed for balancing grows for longer series strings, thereby penalizing both equalization speed and efficiency. Direct balancing architectures overcome this disadvantage by using a common storage component (e.g., a capacitor, inductor, or multi-winding transformer) to transfer energy directly between unbalanced cells, even if they are not adjacent. In theory, the ability of these topologies to transfer energy directly between arbitrary cells can lead to fast equalization speeds and high equalization efficiencies. However, one important limitation is that a direct architecture can typically only balance one pair of battery cells at a time. Therefore, if a pack imbalance scenario involves many cells, the balancing speed of a direct cell-to-cell architecture may deteriorate.

The flying capacitor equalization circuit is one example of direct cell-to-cell equalization [32]. The circuit transfers energy directly from the most-charged cell to the least-charged cell through a so-called "flying capacitor". In theory, this can lead to efficient equalization for cells that are not adjacent to each other in a series string. However, the balancing speeds achieved by this topology are limited by the amount of time needed to charge and discharge the flying capacitor. Another direct cell-to-cell equalization approach is to use an inductor as the intermediate energy storage component, rather than a flying capacitor [33]. Compared to the flying capacitor circuit, this topology can achieve faster equalization. However, this comes at the expense of requiring each battery cell to have two directional delivery channels (i.e., to be able to either charge or discharge through the inductor). This increases the number of switches and diodes required by this topology, which causes the driving circuits in this topology to be badly loaded and reduces equalization efficiency compared to the flying capacitor circuit. Similarly, a direct cell-to-cell equalization method with transformers [34] ensures fast equalization speed but at the cost of a large number of transformers and additional link capacitors.

1.3. Cell-to-pack and pack-to-cell architectures

Cell-to-pack architectures achieve equalization by feeding the excess energy of an over-charged cell back to the entire battery pack [35–37]. In contrast, pack-to-cell architectures transfer energy from the entire battery pack into lower-voltage cells to prevent them from over-discharging [38–40]. These architectures are generally effective at preventing the over-charging or over-discharging of individual battery cells, which is important for pack safety and longevity. Usually, these balancing architectures employ either a fly-back transformer or multi-winding transformer. This creates space limitations: a fact that constrains the number of series-connected cells that can be balanced using these architectures. Moreover, the efficiency of these architectures is limited by two challenges: (i) large voltage stress (i.e., the fact that some of the switches in these architectures operate at pack voltage levels); and (ii) the overlap of energy during balancing (i.e., the fact that some of the energy transferred during the balancing process returns to the same cell from which it is obtained), one exception being the topologies in [41,42].

1.4. Mixed balancing architectures

Given the advantages and limitations of the above balancing circuits, it is reasonable to explore the possibility of combining these circuits into mixed architectures. Examples include the work done by Kutkut et al. the adjacent cell-to-cell and cell-to-pack equalization method [43]; the research done by Du et al. and Chen et al. the cell-to-pack and pack-to-cell equalization method [44–48] and the work presented by Mestrallet et al. the cell-to-pack, pack-to-cell and pack-to-pack equalization method [49] and so on. These structures have the potential to achieve attractive combinations of equalization speed, efficiency, and flexibility. However, the complexity of the underlying circuits and controllers increases significantly with size.

Clearly, none of the above equalization architectures can simultaneously achieve fast equalization speed, high efficiency, and low complexity. In fact, these objectives (equalization speed, efficiency, and simplicity) are fundamentally conflicting, and must therefore be traded off in a systematic manner. The existing literature is quite rich in its analyses of individual balancing architectures, and it also provides qualitative reviews and comparisons between architectures. However, to the best of the authors' knowledge, the problems of (i) developing a formal framework for comparing these architectures quantitatively and (ii) using this comparison for circuit selection and design, remain relatively less explored. The overarching goal of this article is to propose a systematic framework for analyzing different balancing topologies and comparing their balancing speeds and efficiencies. We achieve this goal by using graph theory to represent and analyze different balancing circuit topologies. Graph theory is a science that studies the basic characteristics of interconnected systems by representing their interconnections as "graphs" [50–52]. It is widely used in many areas including the analysis of circuits and electronic networks, but to the best of our knowledge its use for analyzing battery pack balancing circuits is a relatively open research area. One can use graph theory to abstract circuit elements as points and paths. This makes it possible to analyze the performance and efficiency of a given balancing topology without resorting to unnecessarily complex models of the underlying components. Our use of graph theory makes it possible to:

Model different topologies using directed graphs (digraphs).

Represent the efficiencies of different balancing paths in a given topology using a weighted reachability matrix.

Compute the average balancing efficiencies of various single-layer balancing circuits directly from the corresponding weighted reachability matrices.

Perform rigorous comparisons between the expected balancing speeds and efficiencies of different topologies, including both single- and multi-layer topologies.