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Comparative study on different five level inverter topologies

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ABSTRACT

The diode-clamped multilevel topology has the problem of voltage unbalance of dc link capacitors. This can be solved by using separate DC sources, or adding auxiliary circuits or adopting space vector modulation control in three-level inverter applications. For higher level applications, the use of separate DC sources is not viable and the control techniques for other two methods will be more complicated to implement. Hence the Hybrid Multilevel Inverter Based on Switched-Capacitor and Diode-Clamped units can be used for higher levels. This topology can balance the capacitor voltage and also step up the output voltage. The boosting of output voltage contributes to lessen the transformation ratio of the input transformer or even eliminate it, thereby reducing the cost, which will benefit the design of converters in medium–high voltage applications. The topology is simulated using MAT lab simulink software and compared with other voltage balancing techniques.

Introduction

Recently, multilevel inverters [6] have drawn tremendous interest in the field of high-voltage and high-power applications because it can realize high voltage and high power output through low-voltage switches without transformer and dynamic voltage balance circuits, with the number of output level increasing, harmonics of the output voltage and current are decreasing and EM1 are decreasing Multilevel inverters are mainly classified as diode-clamped, capacitor-clamped and cascaded H-bridge inverters.

Among the basic multilevel inverters the problem of voltage unbalance of dc link capacitors exists inherently in the diode-clamped converter topology [13,15], which limits the further application [5] of it, especially at the level above three. To balance the voltage of DC link series capacitors, three main approaches have been proposed. They are: (1) using separate DC sources, [3,7], (2) adding some auxiliary balancing circuits [8,9,16] and (3) improving the control method by selecting redundant switching states, [4,10]. By auxiliary circuits, the transferred current or power can be controlled accurately, but the additional feedback control strategies are also needed, so the control of these converters becomes more complicated, and converters are less reliable.

Voltage balancing techniques

Cascaded H-bridge inverter

A multilevel CHB consists of a number of H-bridge cells connected in series per phase, and each module requires a separate DC source to generate voltage levels at the output of inverter. The output of each bridge is +Vdc, 0 and $-V_{dc}$ and the combinations of the output voltages of series connected bridges give the total output voltage. According to the number of bridges the number of levels of the output voltage changes. The number of bridges is equal to $(n-1)/2$ where n is the number of levels of output voltage. To operate a cascade multilevel inverter [3,7] using a single DC source, it is proposed to use capacitors as the DC sources for all but the first source. Consider a simple inverter with two H-bridges as shown in Fig. 1.

Each H-bridge has a DC power source with an output voltage of V_{dc}. The output voltage of the first H-bridge is denoted by V_1 and the output of the second H-bridge is denoted by V_2 so that the output of this two DC source cascade multilevel inverter is $V = V_1 + V_2$. By opening and closing the switches of H1 and H2 appropriately, the output voltage V_1 and V_2 can be made equal to $+V_{dc}$, 0, or $-V_{dc}$. Therefore, the output voltage of the inverter can have the values, $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$. The firing instants can be obtained by using phase disposition multicarrier PWM technique.

Voltage balancing using resonant switched capacitor converter

Fig. 2 shows a system configuration of a three-phase diode clamped five-level inverter equipped with RSCC voltage balancing

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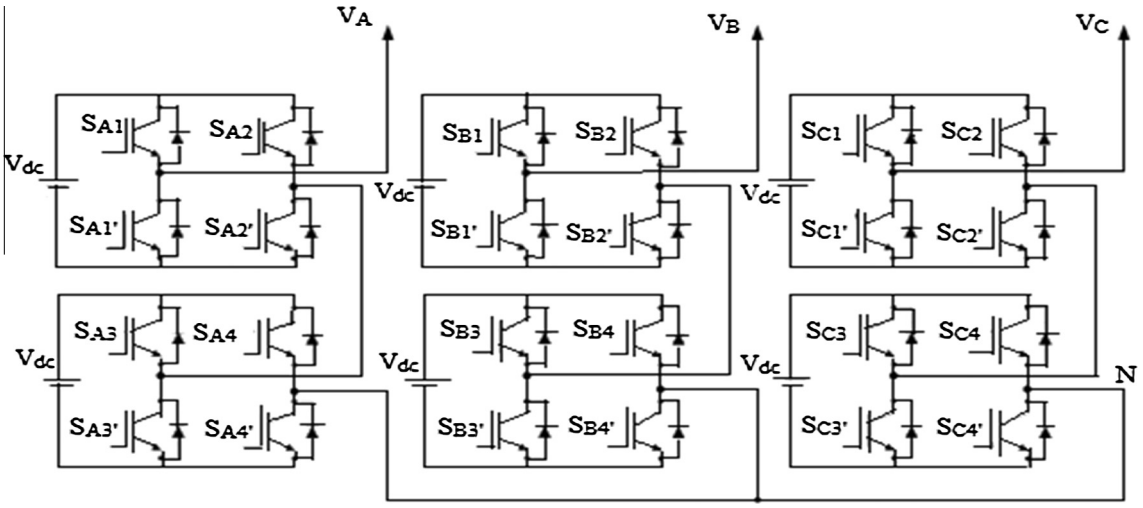

Fig. 1. Five level H-bridge inverter.

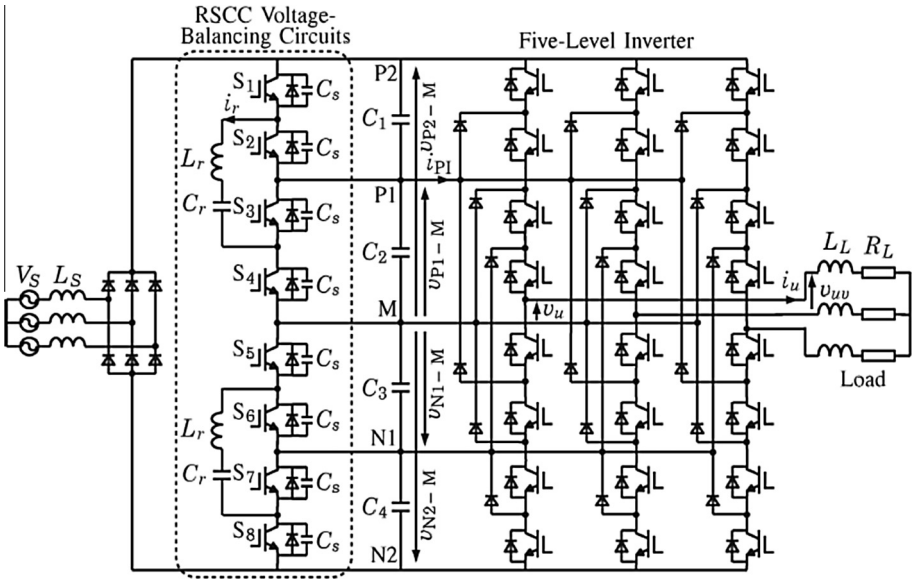

Fig. 2. Five level DCI with RSCC.

circuits [8]. The dc link consists of four dc capacitors C_1–C_4, and it is connected to a three-phase diode rectifier. The rectifier keeps the total voltage across the four dc capacitors as $4V_{dc}$, but each capacitor voltage may deviate from V_{dc}. Therefore, two voltage-balancing circuits are employed to balance their voltages. One is connected to C_1 and C_2, and the other is connected to C_3 and C_4 Symmetrical operation of the five-level inverter makes it possible to maintain the voltage of node M at the center of the dc-link voltage.

While considering the section between P_2 and M, the circuit consists of two half-bridge inverters with four switching devices S_1–S_4 and a series resonant circuit L_r and C_r. The dc terminals of the half-bridge inverters are connected in parallel with the dc capacitor, while an ac terminal is connected to the other one through the series resonant circuit. Dc voltage source $2V_{dc}$ keeps the total capacitor voltage $v_{C1} + v_{C2}$ as $2V_{dc}$. When the v_{C2} decreases by some cause, the dc voltage source supplies an amount of power to both C_1 and C_2, and then v_{C1} increases. The voltage balancing circuit flows a positive current in i_{PB} to discharge C_1 and to charge C_2. The four switching devices enables the bidirectional power flow from C_1 to C_2 or opposite direction. The circuit essentially acts as a switched-capacitor converter or a charge pump circuit, which stores transferred energy in the resonant capacitor C_r, instead of an inductor. The resonant inductor L_r makes it possible to suppress the spike currents, power losses, and electromagnetic noises.

All switching devices are operated with a 50% duty ratio, but their switching frequency is higher than the resonant frequency of the resonant circuit. Therefore, the resonant circuit acts as inductive impedance. The amplitude of the resonant current by means of phase shift between the two half bridge inverters. The proposed method delays S_3 and S_4 from S_1 and S_2 for a phase-shift time T_1. Power P_{rscc} will be maximum when the value of T_1 lies between $-T_{sw}/4$ and $+T_{sw}/4$ where T_{sw} is the time corresponding to the switching frequency of RSCC.

Hybrid Multilevel Inverter Based on Switched Capacitor and Diode Clamped units

The circuit diagram of three-phase topology [1,2] is deduced by combination of three HMI-BSD single-leg circuits sharing common