Neurocomputing 284 (2018) 36–51

Contents lists available at ScienceDirect

Neurocomputing

journal homepage: www.elsevier.com/locate/neucom

Advancing the neurocomputer

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ARTICLE INFO

Article history:
Received 10 July 2017
Revised 21 November 2017
Accepted 8 January 2018

Communicated by Wei Wu

Keywords:
Neurocomputing
Microelectrode arrays
Silicon–neuron interfaces

ABSTRACT

Cultivating neural populations onto microelectrode arrays (MEAs) is a popular technique used by neuroscientists to study cortical microcircuits in a more controlled setting than they appear *in vivo*. However, recent works show that these neural cultures may be more than just another analog to the brain—they can also be used to compute. Researchers in academia and industry may soon need the computing power of a true neuromorphic computer: a silicon computing device that utilizes the processing power of biological neurons. Such a device can be realized by cultivating biological neurons onto an MEA *in vitro* and carefully interfacing the MEA to a computer or robot. This new device can make use of short- and long-term memory mechanisms intrinsic to biological neurons to train neuronal cultures to perform unique computations. Research shows this type of computing device may be able to solve problems in fields like image recognition, temporal pattern classification, and others. In this paper, we review the methods of interfacing cultures with MEAs, learning mechanisms exhibited in neuronal cultures, the current applications of a neuron–silicon hybrid computing device in research, and potential challenges this field may face. We propose that the current research in neurocomputers has provided the foundations for a new era in computing, one in which the computational power of true biological neural networks may be exploited and eventually surpass the power of artificial neural networks.

1. Introduction

Artificial Intelligence (AI) is an interdisciplinary field with the goal of imitating the computational versatility of human intelligence with silicon technology. Neural networks composed of real or simulated neurons are capable of this flexibility and can solve computationally difficult problems like pattern recognition and classification [46]. However, simulating large neural networks with traditional computers has proven challenging due to the huge computational resources required.

One approach to solve this problem is to incorporate biological neurons into silicon technology to create a neurocomputer—a hybrid silicon-tissue computing machine that utilizes the processing power of biological neurons to perform computations on an input. Biological neurons can effortlessly make numerous interconnections between themselves and adapt those connections through Hebbian learning [43]. These advantages could be utilized in a neurocomputer to perform the same computations while sparing the resources required to simulate neurons like in a recurrent neural network.

This new computational paradigm provides its own unique challenges in areas such as device design and understanding of neural cultures. However, these neurocomputers may have some niche applications to traditionally incomputable problems, such as how DNA computing solved the Hamiltonian path problem [3]. Neurocomputers have shown promising results in the fields of spatiotemporal pattern classification [14,27,53,54], simple image recognition [82], and liquid-state computing [26,71]. The purpose of this paper is to explore and assemble a body of research that could aid in the advancement of the neurocomputer.

Within the scope of this paper, we explore key technologies which may prove pivotal in designing an interface to communicate between the silicon-instantiated and neuron-instantiated computational components, including silicon chip interfaces, complementary metal-oxide semiconductor (CMOS) interfaces, two-dimensional (2D) microelectrode arrays (MEAs), improving biosimilarity between the two components, and three-dimensional (3D)

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https://doi.org/10.1016/j.neucom.2018.01.021
0925-2312/

neural cultures. Then, we explore the basic neural mechanisms which a neurocomputer would exploit to train the neural component of the device. We provide a brief history of the young field and explore notable applications of the technology, and close with challenges and future directions of the field.

2. Methods

2.1. Interfaces

Central to the design of the neurocomputer is the process of interfacing between the neuron and silicon components of the device. By sending specific stimuli to the neural network, it is possible to condition the network and teach the biological system to perform computations using neural learning mechanisms such as long-term potentiation (LTP) [82]. Alternatively, activity from the neural network can be measured and sent to the silicon-instantiated computer. Both the input and output process of the neurocomputer is dependent on the design of the interface.

In device design, the main challenges revolve around neuron–electrode interfaces: (i) connections made onto the cultivated neural networks in today's technology are significantly less complex compared to the human brain; (ii) there exists a limit in the complexity of biological neural network design; (iii) small volume size in electrodes must be maintained to minimize tissue damage, but recording sites must be large enough to maintain signal integrity; and (iv) the neuron–electrode interface must be biocompatible over long periods of time. These issues will be explored throughout this review.

Methods for intracellular recordings of neuron membrane potentials have been around for decades [10,94]. Early neuron recordings involved maneuvering a sharp electrode with a micromanipulator to penetrate a cell membrane and make physical contact with the cytosol [41]. This method of recording provides great coupling with selective single cell stimulation while generating reliable data [89]. However, due to the bulky size of the micromanipulator and the biophysical instability of the electrode-cell interface, this method of recording can only be done on a small number of neurons for a short time, which significantly limits any potential applications to the multi-cell circuits involved in neurocomputing [9,31].

Substrate-integrated MEAs are more popular for extracellular recordings of larger neural circuits [44]. In most MEA recording experiments, cells are seeded onto a bed of electrodes and allowed to grow into a circuit with either random or directed connections between neurons [41]. MEAs are capable of measuring extracellular activity of more than 10,000 individual neurons by using thousands of electrodes [40,64,87]. This design provides a high temporal resolution and enough spatial resolution to detect single action potentials even within synchronized bursts [41].

However, there are interfacing techniques which may prove useful in the development of a neurocomputer and which diverge from common MEA techniques, such as silicon chip interfaces and CMOS integrated interfaces. This section will review these techniques as well as MEA technology.

2.1.1. Silicon chip interfaces

Unique from MEAs, silicon chip interfaces can be constructed by taking two disconnected neurons (in [13], cultivated from the pedal ganglia of the pond snail Lymnaea stagnalis) and attaching them onto the silica surface of a microstructured chip (shown in Fig. 1(B)) to perform non-invasive electronic recording and stimulation [13]. This technique eschews the use of an MEA entirely in favor of a microstructured silicon chip. The entire pathway of the hybrid neuron silicon chip can be broken down into five stages: (1) recording neural activity from the first neuron by the first contact, (2) translating the neural signal to a digital signal, (3) sending the digital signal through a delay line, (4) triggering a voltage pulse in the second contact and (5) eliciting an action potential from the second neuron by the second contact.

The microstructured chip is a two-unit system; one unit interfaces the neurons and the other unit processes the signal (Fig. 1(A), left subplot). Two neurons are placed on top of a two-way interface contact (shown in Fig. 1(B)). The left contact is called a transistor while the right is called a capacitive stimulator (Fig. 1(B), left subplot). The transistor consists of a boron doped source and drain channel and a gate channel covered with a non-metal oxide, while the capacitive stimulator is boron-doped (Fig 1(A), right subplot). The role of the transistor is to detect the firing of an action potential within *Neuron A*, and then transform the response to a digital signal to be sent across the delay line. The signal then triggers a burst of voltage pulses that is applied to the capacitive stimulator. The capacitive stimulator elicits an action potential from *Neuron B*. The two units are then bonded side-by-side beneath a Perspex chamber. The chamber is designed to hold the cell culture medium where the interfacing unit comes in contact with the culture medium (Fig. 1(C), right subplot).

The circuit model of the neuron–silicon chip–neuron pathway is shown in the left subplot of Fig. 1(C), where the upper portion shows the equivalent circuit of the neuron–silicon coupling. The capacitance forming around the neuron is due to its surroundings and the interface. The lower portion illustrates the block circuit diagram of the electronic processor, both the transistor and capacitive stimulator. The cells are separated from the chip by a narrow film of electrolyte with low conductance to increase the biocompatibility of the device.

This device shows that on a microscopic level, an action potential generated from an individual neuron can be sent to a digital electronic processor, and a simple capacitive stimulator can elicit an action potential from an individual neuron [13]. Expanding this technology to interface whole neuronal cultures in a neurocomputer would be challenging. However, advancements in this technology may allow direct, lossless communication between individual neuron and neuron populations across long distances while avoiding the intricacies involved in creating long-distance neural connections via axons. These connections could be used for connecting multiple layers of networks required in pattern recognition and other complex computations.

2.1.2. Interfacing using CMOS circuits

In addition to using silicon chip interfaces, researchers developed a double-sided, single-chip device that integrates CMOS circuits with micro-electro-mechanical system (MEMS) structures through the use of through-silicon via (TSV) electrical connections. A TSV is an electrical connection that passes through the entire double-sided device in order to send information from the CMOS to the MEMS section while avoiding degradation of the signal (Fig. 2) [17]. The redistribution layers (RDL) placed on the front side of the chip serve to create a connection between the CMOS circuit and TSVs.

This new approach integrates various technologies, (*i.e.* CMOS, MEMS, nanoelectronics, *etc.*) in order to advance neural sensing, processing, networking, and developing neural prosthetics [17]. While this device was developed to serve as a neural implant with a smaller footprint, this technology could also serve as an interface between the neural and silicon components of a neurocomputer. The device collects more information from a smaller, more specific neural population and avoids interference from surrounding circuits. In addition, due to the layout of the double-sided integrated chip, the device uses area efficiently which results in a smaller neurocomputer [17].