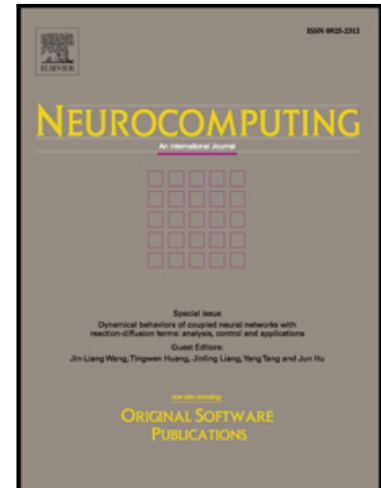


Accepted Manuscript

Memristive Recurrent Neural Network

Gerardo Marcos Tornez Xavier , Felipe Gómez Castañeda ,
Luis Martín Flores Nava , José Antonio Moreno Cadenas

PII: S0925-2312(17)31355-3
DOI: [10.1016/j.neucom.2017.08.008](https://doi.org/10.1016/j.neucom.2017.08.008)
Reference: NEUCOM 18745



To appear in: *Neurocomputing*

Received date: 8 November 2016
Revised date: 5 August 2017
Accepted date: 7 August 2017

Please cite this article as: Gerardo Marcos Tornez Xavier , Felipe Gómez Castañeda , Luis Martín Flores Nava , José Antonio Moreno Cadenas , Memristive Recurrent Neural Network, *Neurocomputing* (2017), doi: [10.1016/j.neucom.2017.08.008](https://doi.org/10.1016/j.neucom.2017.08.008)

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

Memristive Recurrent Neural Network Author Names and Affiliations

Gerardo Marcos Tornez Xavier^a
Felipe Gómez Castañeda^a
Luis Martín Flores Nava^a
José Antonio Moreno Cadenas^a

^aCenter for Research and Advanced Studies of the IPN, Cinvestav-IPN,
Electrical Engineering Department,
Av. Instituto Politécnico Nacional 2508,
CP 07360, Mexico City, Mexico

e-mail: {gtornez, fgomez, lmflores, jmoreno}@cinvestav.mx

Corresponding Author

Dr. Felipe Gómez Castañeda
e-mail: fgomez@cinvestav.mx

Abstract

It is reported a continuous-time neural network in CMOS that uses memristors. These nanodevices are used to achieve some analog functions such as constant current sourcing, decaying term emulation, and resistive connection; all of them representing parameters of the neural network. The expected dynamics of this silicon circuit with these functional memristors is demonstrated via SPICE simulations based on 0.5-micron, n-well CMOS technology. The neural circuit is operative by finding the optimal solution of small-size combinatorial optimization problems, namely: "Assignment" and "Transportation". It was chosen fast switching titanium dioxide memristors, which are modeled with nonlinear window functions and tunneling effect with the TEAM paradigm. This analog network belongs to an early recurrent model, which is electrically redesigned to take into account memristive arrays but keeping its original convergence properties. The behavioral and electrical analysis is done via Simulink-SPICE simulation. The outcome VLSI functional blocks combine both current and voltage to represent the variables in the recurrent model.

Key Words:

Memristor; TEAM Model; Neural Network; Hopfield; Continuous-Time Signal; Analog VLSI Design

Introduction

Download English Version:

<https://daneshyari.com/en/article/6865105>

Download Persian Version:

<https://daneshyari.com/article/6865105>

[Daneshyari.com](https://daneshyari.com)