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Brief Papers

Emulation of spike-timing dependent plasticity in nano-scale phase change memory

Dae-Hwan Kang [a], Hyun-Goo Jun [a], Kyung-Chang Ryoo [a], Hongsik Jeong [b,*], Hyunchul Sohn [c]

[a] Memory Division, Semiconductor Business, Samsung Electronics Co. Ltd., 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-Do 445-330, Korea
[b] Yonsei Institute of Convergence Technology, Yonsei University, 85 Songdogwahak-ro, Yeonsu-gu, Incheon 406-840, Korea
[c] Department of Materials Science and Engineering, Yonsei University, Seoul 120-749, Korea

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ABSTRACT

The spike-timing dependent plasticity (STDP) of biological synapses, which is known to be a function of the formulated Hebbian learning rule of human cognition, learning and memory abilities, was emulated with two-phase change memory (2-PCM) cells built with 39 nm technology. For this, we designed a novel time-modulated voltage (TMV) scheme for changing the conductance of 2-PCM cells, that could produce both long-term potentiation (LTP) and long-term depression (LTD) by applying variable (decreasing/increasing) pulse voltages according to the sign and magnitude in time interval between pre- and post-spikes. Since such schemes can be easily modified to have a variety of pulse shapes and time intervals between pulses, it is expected to be a proper scheme for designing diverse synaptic connection abilities. In addition, the small form factor and low energy consumption of 2-PCM make them comparable to biological synapses, which makes phase change memory a promising candidate for electronic synapses in large-scale neuromorphic system applications.

1. Introduction

The term neuromorphic engineering, which was coined by Carver Mead [1], has given rise to significant progress in the uprising application fields of brain-inspired computing, smart sensors, and associate memory, which is based on CMOS analog, digital and/or combined circuits, called silicon neural networks (SiNs). These networks mimic the information processing pathways of biological neurons such as signal reception, propagation, transference to neighboring neurons, and storage [2–4].

Fig. 1(a) shows a schematic of biological neurons and the synapses in-between, where it is known that signal receipt and transmission are achieved by the generation of action potentials in soma and its propagation along the axons of the neuron, respectively (neuron spiking). Meanwhile, signal transfer and storage are determined by the connection strength of the synapses between neurons (synaptic plasticity). In particular, synaptic plasticity, or the change in synapse connectivity, is widely believed to underlie our learning processes and memory. Though there have been some reports [5–7] of mimicking synaptic plasticity using SiNs, they are somewhat inappropriate for practical use in large scale neuromorphic applications, because of the large consumption of area and power of complicated circuits.

Following the famous hypothesis of a Canadian psychologist [8] on synaptic plasticity, it is expected that the connectivity in between synapses will change plastically when two neighboring neurons spike temporally together. A representative algorithm for such a hypothesis is briefly depicted using three neurons in Fig. 1 (a), synaptic strengths may change depending on the relative timing of pre- and post-synaptic spikes. The synaptic strength is potentiated (or strengthened) if pre-spike A precedes post-spike B ($\Delta t > 0$) whereas it is depressed (or weakened) if pre-spike A follows post-spike C ($\Delta t < 0$). Such a timing algorithm in synaptic strength's modification or change is called spike-timing dependent plasticity (STDP) [2]. In other words, the change in synapse strength (ΔC) is positive (the synaptic connectivity is potentiated) when $\Delta t > 0$, and it becomes higher at smaller Δt, which is called long-term potentiation (LTP). Meanwhile, ΔC is negative (the synaptic connectivity is depressed) when $\Delta t < 0$ and it becomes more negative at smaller negative Δt, which is long-term depression (LTD), as seen in Fig. 1(b).

In this study, we introduce a novel scheme for emulating STDP which is easily applicable to any nano-scale memory device when

* Corresponding author. Tel.: +82 32 749 5845; fax: +82 32 818 5801.
E-mail addresses: daehwan.kang@samsung.com (D.-H. Kang), h9.jun@samsung.com (H.-G. Jun), Kc.ryoo@samsung.com (K.-C. Ryoo), hongsik.jeong@yonsei.ac.kr (H. Jeong), hyunchul.sohn@yonsei.ac.kr (H. Sohn).

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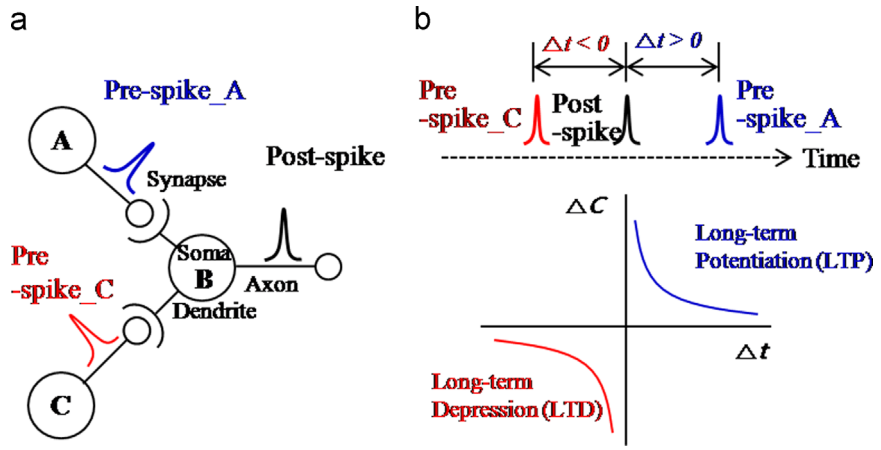

Fig. 1. (a) The schematic of biological neurons and (b) the spike-timing dependent plasticity (STDP) showing long-term potentiation (LTP) and long-term depression (LTD) according to the time-interval between the pre- and post-spikes.

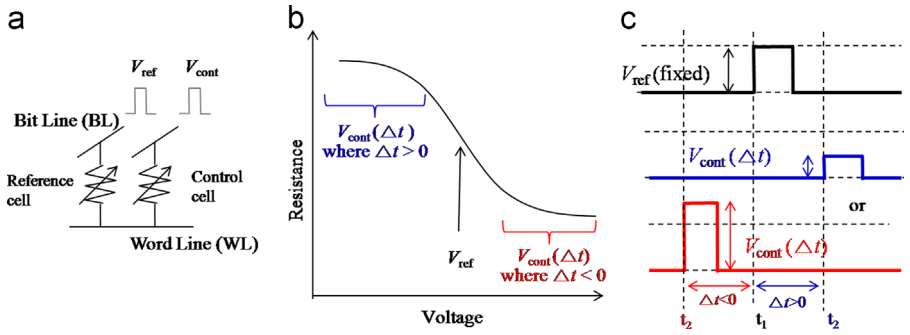

Fig. 2. (a) Schematic of two resistive memory cells, where V_{ref} and V_{cont} are pulse voltages to reference and control cells, respectively. (b) Concept of time-modulated voltage ranges in typical *R-V* analog curve with respect to the time interval between spikes of pre-synaptic and post-synaptic neurons (Δt). (c) The voltage timing diagram, where blue and red texts respectively correspond to LTP and LTD cases.

if having analog resistance behavior with respect to external stimuli. For an experimental verification of this scheme, we emulated STDPs in two-phase change memory (2-PCM) cells made with 39 nm technology by introducing a novel time-modulated voltage (TMV) pulse scheme. Various STDP shapes can be easily obtained by varying the shape of voltage pulses and the time interval between two cells, which helps to design diverse synaptic connection abilities.

2. Concept for STDP emulation in two resistive memory cells

To emulate the STDP of one synapse, we can take into account two resistive memory cells which are connected to pre-synaptic and post-synaptic neurons through their respective bit lines, as shown in Fig. 2(a). One is a reference cell with a fixed resistance and the other is a control cell with variable resistances. After the reset initialization for two cells to be high resistance, independent voltage pulses called set pulses are applied, based on the intrinsic *R–V* curve of Fig. 2(b), to reduce the resistance of the two cells. It should be designed that the set voltage is fixed for the reference cell (V_{ref}) to have always an intermediate resistance whereas the set voltage to control cell (V_{cont}) is modulated to have various resistance levels so that the two cells have different resistance values with respect to the time interval between the spikes of the pre-synaptic and post-synaptic neurons (Δt). As depicted in Fig. 2(c), in the case of $\Delta t > 0$, V_{cont} is set to be inversely proportional to Δt whereas in the case of $\Delta t < 0$, V_{cont} is set to be proportional to Δt. Then, when the reciprocal of the resistance difference of the two cells is considered as the conductance change (ΔC) and it is plotted with Δt, we can obtain an STDP shape.

3. Experiment

For a representative demonstration of the scheme suggested above, we emulated STDP behaviors by making use of two PCM cells, using state-of-the-art 39 nm technology. As shown in Fig. 3(a), a PCM cell has a p–n diode switch epitaxially grown on an N+ Si word line (WL), ring-type bottom electrode (BE), a damascene-type $Ge_2Sb_2Te_5$ (GST) phase change material, line-type top electrode (TE) and bit line (BL). Fig. 3(b) represents the circuit diagram of 2-PCM cells with two-channel pulse generator which can generate two independent pulses with a time interval as precise as 10 ns. In addition, Fig. 3(c) and (d) depict the block diagram of a programming algorithm, and the detailed pulse conditions and their expected resistance change with respected to the sign of Δt.

First, both reference and control cells have high resistance values of several MΩ (R_{init}), using an initial short pulse of 5 V height with a 10 ns-rise, 80 ns-duration, and 10 ns-fall. Then, we make a reference cell to induce a few hundred kΩ (R_{ref}) by applying the fixed voltage of 5 V with a 100 ns-rise, 50 ns-duration, and 100 ns-fall widths at time t_0. Next, we apply a time-modulated voltage (TMV) at time $t_0+\Delta t$ for a control cell to have various resistance values (R_{cont}) according to the sign and magnitude of Δt. Here, we use a 5 V - (5 V/Δt_{max}) × Δt pulse height as a TMV example under the same pulse widths and repeat to write a control cell with an increase of Δt from 1 ms to 20 ms, as described in Fig. 3(c).

4. Emulation of STDP in two-phase change memory cells

Fig. 4(a) shows resistance changes in reference and control cells (R_{ref} and R_{cont}) with respect to Δt, which has resulted from the