Using well-solvable quadratic assignment problems for VLSI interconnect applications

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A B S T R A C T

This paper presents several optimization problems occurring in VLSI interconnect, Networks on Chip (NoC) design and 3D VLSI integration, all possessing closed-form solutions obtained by well-solvable Quadratic Assignment Problems (QAP). The first type of problems deals with the optimal ordering of signals in a bus bundle such that the switching power, delay and noise interference are minimized. We extend a known solution of ordering the signals in a bus bundle to minimize the impact of the first order wire-to-wire parasitic capacitance occurring between adjacent wires into a model accounting for also secondary components of wire-to-wire parasitic capacitances. The second type of problems arises in the mapping of computation tasks into an array of processors sharing a common bus, such as those found in NoC. We show a QAP closed-form solution to the optimal mapping problem which simultaneously minimizes the switching power and the average delay of the bus. The third problem deals with the optimization of 3D VLSI, vertically stacking ordinary ICs. Some of the above problems involve *k*-salesmen Traveling Salesman Problem (TSP), where costs are evaluated for elements located at *k*-distance apart along the tour. We show a simple proof that these are well-solvable problems and obtain their solution. This is then generalized to well-solvable QAPs obtained by superposition of such TSPs. A simple proof shows that if *k*-distance TSPs are well-solvable, so is the QAP obtained by their sum, where the solution of 1-distance TSPs dominates all the others.

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1. Introduction

In the following, we present three types of problems occurring in VLSI circuit and system design, and their relation to Traveling Salesmen Problem (TSP) and Quadratic Assignment Problem (QAP). TSP and QAP are well known intractable problems, but there are special instances where TSP [9,4,6] and QAP [21,3,7,17] are well-solvable. In the following, we show that those VLSI problems are mapped into well-solvable TSPs and QAPs.

1.1. Minimizing delay and dynamic power in VLSI interconnect bus bundle

Fig. 1a illustrates a commonly used *n*-wire bus bundle. There, logic gates called drivers drive signals propagating along interconnecting wires. These signals stimulate other logic circuits, called receivers, connected at the opposite end of the wires. The bus is shielded by wires connected to ground. Cross-coupling parasitic capacitance (cross-cap for short) which is a predominant cause of signal propagation delay, dynamic (switching) power consumption and crosstalk noise interference,
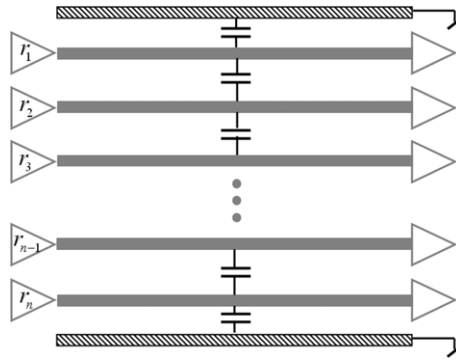
Fig. 1a. Typical VLSI interconnect bus. Drivers are shown on the left side and receivers on the right side. The bus is shielded on its two sides. A parasitic cross-coupling capacitance is incurring between any adjacent signals.
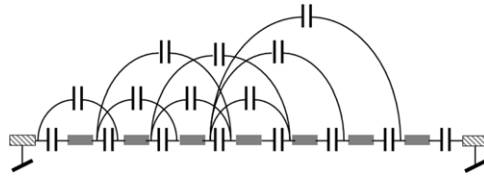

Fig. 1b. Cross-section of a 7-signal shielded bus. All line-to-line cross-coupling capacitances are shown (1-distance). Few other 2-distance, 3-distance and 4-distance capacitances are also shown.

occurs between any two wires of the bus [1]. The primary component of the cross-cap is occurring between adjacent wires, where we say that the wires are at 1-distance of each other. Secondary cross-cap components exist in the bus as shown in Fig. 1b. Most interconnect optimization algorithms account for only 1-distance cross-cap, which is claimed to reach 90% of the total cross-cap. A secondary component of about 6% is due to wires at 2-distance and the rest are due to higher distances. The secondary cross-cap impact on power dissipation and the accuracy of power estimation were studied in [15]. The question of how to order the wires in the bus to yield best performance (dynamic power consumption, delay and noise immunity) has been studied for 1-distance cross-cap, and it was shown to be a well-solvable TSP [20]. It is shown in the sequel that accounting for secondary cross-cap components results in a well-solvable QAP, which generalizes the former result.

A well known VLSI optimization problem is the setting of wire widths and spaces in a bus bundle whose total width (the distance between the shields in Fig. 1a) is constrained [19]. The question of how to order the wires in the bus such the above optimization will yield best bus performance was discussed in several works [13,12,18,10,8,22], where at each paper focused on a single objective, an all considered only 1-distance cross-cap. We show subsequently that the consideration of secondary cross-cap does not change the optimal order of wires in the bus. Accounting for a k-distance component alone, $1 \leq k \leq n-1$, implies a sort of TSP with k salesmen. Considering all distances simultaneously yields a special QAP, which is a sum of all k salesmen TSPs. We show in Section 3 that in the combined problem the 1-distance solution, corresponding to the ordinary TSP (one salesman), dominates all the others.

Bus modeling associates with every wire a parameter r whose meaning depends on the optimization problem of interest. For delays r is the resistance of the signal's driver. For dynamic power consumption and noise interference r represents signal's relative switching probability, called activity factor in VLSI jargon [11]. Given an arbitrary order of the wires in the bus, let n real nonnegative parameters $r_1, \ldots, r_n$ be associated with the wires. It was shown in [13,12,18,10,8,22] that up to a multiplicative factor which is independent of problem's setting, once the widths and the spaces are set to minimize delay, dynamic power or noise interference, the objective function satisfies the following expression:

$$F(r_1, \ldots, r_n) = \sqrt{r_1} + \sum_{i=1}^{n-1} \sqrt{r_i + r_{i+1}} + \sqrt{r_n}. \tag{1.1}$$

In [18] the minimization of noise interference between signals was considered. In [13] average delay of a signal was the minimization objective and in [12,10,8,22] dynamic power minimization was addressed.

Eq. (1.1) rouses the question of what is the order of wires among all the $n!$ possible permutations which minimizes F. For convenience, expression (1.1) can be modified into a cyclic sum by adding two artificial parameters $r_0 = r_{n+1} = 0$, turning it into $F(r_0, r_1, \ldots, r_n, r_{n+1}) = \sum_{i=0}^{n+1} \sqrt{r_i + r_{i+1}}$, where $n + 2 \stackrel{\Delta}{=} 0$. To adhere the indexing commonly used in combinatorial