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On the parameterized complexity of monotone and antimonotone weighted circuit satisfiability ☆

Iyad Kanj [a,*], Dimitrios M. Thilikos [b,1], Ge Xia [c]

[a] School of Computing, DePaul University, 243 S. Wabash Avenue, Chicago, IL 60604, USA
[b] Department of Mathematics, National and Kapodistrian University of Athens, Greece and AlGCo project team, CNRS, LIRMM, France
[c] Department of Computer Science, Acopian Engineering Center, Lafayette College, Easton, PA 18042, USA

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ABSTRACT

We consider the weighted monotone and antimonotone satisfiability problems on normalized circuits of depth at most $t \geq 2$, abbreviated WSAT$^+[t]$ and WSAT$^-[t]$, respectively, where the parameter under consideration is the weight of the sought satisfying assignment. These problems model the weighted satisfiability of monotone and antimonotone propositional formulas, and serve as the canonical problems in the definition of the parameterized complexity hierarchy. Moreover, several well-studied problems, including important graph problems, can be modeled as WSAT$^+[t]$ and WSAT$^-[t]$ problems in a straightforward manner.

We study the parameterized complexity of WSAT$^-[t]$ and WSAT$^+[t]$ with respect to the genus of the underlying circuit. We give tight results, and draw a map of the parameterized complexity of these problems with respect to the genus of the circuit. As a byproduct of our results, we obtain tight characterizations of the parameterized complexity of several problems with respect to the genus of the underlying graph.

1. Introduction

We consider the *weighted satisfiability* problems on monotone and antimonotone normalized circuits of depth at most $t \geq 2$. In the ANTIMONOTONE WEIGHTED SATISFIABILITY problem on normalized circuits of depth at most $t \geq 2$, abbreviated WSAT$^-[t]$, we are given a circuit C of depth t in the *normalized* form [12,13] (*i.e.*, the output gate is an AND-gate, and the gates alternate between AND-gates and OR-gates) whose input literals are all negative, and an integer parameter $k \geq 0$, and we need to decide if C has a satisfying assignment of weight k (*i.e.*, assigning the value 1 to k variables of C). In the MONOTONE WEIGHTED SATISFIABILITY on normalized circuits of depth at most $t \geq 2$, abbreviated WSAT$^+[t]$, we are given a circuit C of depth t in the normalized form whose input literals are positive, and an integer parameter $k \geq 0$, and we need to decide if C has a satisfying assignment of weight k. Our goal in this paper is to study the parameterized complexity of WSAT$^-[t]$ and WSAT$^+[t]$ with respect to the genus of the circuit. We define the genus of the circuit to be the genus of

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* Corresponding author.
E-mail addresses: ikanj@cs.depaul.edu (I. Kanj), sedthilk@thilikos.info (D.M. Thilikos), gexia@cs.lafayette.edu (G. Xia).

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the underlying undirected graph after the output gate is removed. The reason we exclude the output gate of the circuit in the definition of the genus is two-fold. First, excluding the output gate allows us to use standard FPT-reductions to model problems on graphs satisfying a certain genus upper bound as WSAT$^-[t]$ and WSAT$^+[t]$ problems on circuits that satisfy the same genus upper bound, whereas such modeling would not be possible if the genus is defined to be that of the whole circuit. Second, as it turns out, one obtains the same tight results obtained in the current paper if the genus is defined to be that of the whole circuit. To see this, observe that all positive results (FPT membership results) obtained in this paper carry over because an upper bound on the genus of the whole circuit implies the same upper bound on the genus of the same circuit with the output gate removed. Therefore, showing that the WSAT$^-[t]$ and WSAT$^+[t]$ problems are FPT on circuits whose genus defined with the output gate removed is at most $g(n)$, for some function $g(n)$, where n is the number of variables in the circuit, will imply that the WSAT$^-[t]$ and WSAT$^+[t]$ problems are FPT on circuits whose genus defined with the output gate included is at most $g(n)$. On the other hand, the same straightforward (padding) arguments used to obtain the W-hardness results in this paper (Lemmas 3.5 and 4.2) with the genus defined after removing the output gate, can be used to obtain W-hardness results for the same upper bound on the genus when the genus is defined to be that of the whole circuit. We mention that the WEIGHTED CIRCUIT SATISFIABILITY problem on depth-t planar circuits with the output gate included is solvable in polynomial time [7], whereas it can be easily shown that WSAT$^-[t]$ and WSAT$^+[t]$ are NP-complete on planar circuits (and hence on circuits of any genus) with the output gate removed. We also note that WEIGHTED CIRCUIT SATISFIABILITY on planar circuits with unbounded depth is known to be W[P]-complete [1]. Recently, in [23], Marx proved that weighted monotone/antimonotone circuit satisfiability has no FPT-approximation algorithm with any approximation ratio function ρ, unless W[1] = FPT.

1.1. *Motivation and related work*

The problems under consideration are of prime interest both theoretically and practically. From the theoretical perspective, they naturally represent the weighted satisfiability of (monotone/antimonotone) t-normalized propositional formulas, *i.e.*, products-of-sums-of-products... (see [12,13]), including the canonical problems weighted antimonotone/monotone CNF-SAT. Moreover, the WSAT$^-[t]$ and the WSAT$^+[t]$ problems are the canonical complete problems for the different levels of the parameterized complexity hierarchy – the W-hierarchy, and the W-hierarchy can be defined based on them [12,13]. Therefore, determining the underlying structure that makes these problems (parameterized) tractable is important from the perspective of complexity theory. From a more practical perspective, WSAT$^-[t]$ and WSAT$^+[t]$ can model several natural problems. Therefore, parameterized algorithms for WSAT$^-[t]$ and WSAT$^+[t]$ can be used to obtain parameterized algorithms for some natural problems via FTP-reductions to/from WSAT$^-[t]$ and WSAT$^+[t]$, as we shall see in Section 5.

The computational complexity of many natural problems on planar graphs, and more generally on graphs whose genus meets certain upper bounds, have been extensively researched (see [4,9,10,15,16], among others). In particular, it was shown that the bounded-genus property plays a key-role in determining the computational complexity (parameterized complexity including kernelization, subexponential-time computability, and approximation) of a large class of graph problems. For example, using *bidimensionality theory*, it was shown in [9] that a large class of graph problems admit subexponential-time parameterized algorithm on graphs whose genus is upper bounded by a constant. For graphs of larger genus (could be unbounded), it was shown in [8] that the genus characterizes the computational complexity (parameterized complexity, approximation, and subexponential-time computability) of some natural graph problems, including INDEPENDENT SET and DOMINATING SET. We note that the techniques used in [8] to characterize the parameterized complexity of certain graph problems with respect to the genus of the graph are problem specific, and are not applicable to the weighted satisfiability problems under consideration in this paper.

Research results on planar circuits, and on satisfiability problems defined on certain structures that are planar or that satisfy certain structural properties, are abundant. Planar Boolean circuits have been extensively studied in the literature as they can be used to study VLSI chips, and they play an important role in deriving computational lower bounds for Boolean circuits [24,26,28]. After Lipton and Tarjan established their celebrated planar separator theorem, one of the first applications of the separator theorem they gave, was to derive lower bounds on the size of Boolean circuits that compute certain important functions [22]. The computational power of monotone planar circuits were also considered (*e.g.*, see [2,21]). Khanna and Motwani [19] studied the approximation of instances of satisfiability problems (weighted and unweighted) whose underlying structure is planar. More specifically, they studied satisfiability problems defined based on disjunctive normal form (DNF) formulas. The incidence graph of an instance of such problems is a simple bipartite graph that has a vertex for each variable and a vertex for each formula, and an edge between them if the variable occurs in the formula. They derived polynomial-time approximations schemes for instances of these problems whose underlying incidence graph is planar [19]. Cai et al. [6] studied the parameterized complexity of the satisfiability problems introduced by Khanna and Motwani [19], and showed that these problems are W[1]-hard even when the underlying incidence graph is planar. Researchers have also studied the parameterized complexity of CNF-SAT with respect to the treewidth of a graph defined by the corresponding formula (for example, see [25]).