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A note on monotone real circuits [‡]

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1. Introduction

In this note, we present some structural properties of the computational model of monotone real circuits. Motivated by proof complexity applications, monotone real circuits were introduced in [10] where an exponential lower bound was obtained for this model; a similar lower bound was independently obtained in [3]. The first issue we address here is the arity of gates used in computation. Monotone real circuits, in their usual definition, use binary (and unary) gates over the reals. But if we allow, say, ternary gates, can we significantly speed-up the computation? For Boolean circuits, or circuits involving functions over a finite domain, the answer is obvious: every ternary gate can be expressed as a composition of a constant number of binary gates, so using ternary gates can give an advantage of at most a constant factor. In the case of computations over the reals, or any infinite ordered set, an analogous statement is far from obvious. In [2], the possibility of

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ABSTRACT

We show that if a Boolean function $f : \{0, 1\}^n \to \{0, 1\}$ can be computed by a monotone real circuit of size *s* using *k*-ary monotone gates then *f* can be computed by a monotone real circuit of size $O(sn^{k-2})$ which uses unary or binary monotone gates only. This partially solves an open problem presented in [2]. In fact, in size $O(sn^{k-1})$, the circuit uses only unary monotone gates and binary addition. We also show that if the monotone Karchmer–Wigderson game of *f* can be solved by a "real communication protocol" of size *s* then *f* can be computed by a monotone real circuit of the same size.

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gate-by-gate by simulation was stated as an open problem. We don't know how to solve this problem, but we nevertheless show that ternary gates, or gates of not too large an arity, indeed cannot substantially speed-up real computations. We also show that the only gates needed are monotone unary gates and binary additions. This is interesting in comparison with Kolmogorov's superposition theorem [1,8] which states that every k-ary continuous function can be expressed using unary continuous functions and addition.

Second, we give a correspondence between monotone real circuits and real communication protocols. This resembles a similar correspondence between Boolean circuits and PLS-based protocols of Razborov [12], and, more closely, the construction of Krajíček [9] (see also [11,13]). The motivation is the following. In [7], Karchmer and Wigderson characterized Boolean circuit depth in terms of deterministic complexity of certain communication games. This game-theoretic viewpoint has been very useful both in proving lower bounds and constructing upper bounds on circuit depth. The constructions in [12,9] are intended to give a similar interpretation of Boolean circuit size in terms of games. This is useful especially when proving feasible interpolation theorems in various proof systems. We now give a similar characterization of monotone real circuits in terms of real games. As in [9] or [11], such a characteriza-

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tion can be directly used to give a simple proof of feasible interpolation in the Cutting Planes proof system, or applied to the related notion of "unsatisfiability certificates" introduced in [6].

2. Monotone real circuits of high fan-in

For $x, y \in \mathbb{R}^n$, we write $x \le y$ if $x_i \le y_i$ for every coordinate $i \in [n] = \{1, ..., n\}$. A function $f : S \subseteq \mathbb{R}^n \to \mathbb{R}$ will be called *monotone*, if for every $x, y \in S, x \le y$ implies $f(x) \le f(y)$. We remark that, assuming $\sup\{|f(x)| : x \in S\} < \infty$, f is monotone iff it is a restriction of some *total* monotone function $g : \mathbb{R}^n \to \mathbb{R}$. Since we will usually deal with a finite *S*, the distinction between partial/total functions is hence quite unimportant.¹

A *k*-ary monotone real circuit is a finite directed acyclic graph with every node of in-degree at most *k*. It has one output node of out-degree zero. Nodes of in-degree zero are called input nodes and are labeled with variables. Every other node *v* of in-degree *p* is labeled with a (total) monotone function $g_v : \mathbb{R}^p \to \mathbb{R}$. The size of the circuit is the number of its gates. The circuit computes a function $f : \mathbb{R}^n \to \mathbb{R}$ in the obvious way: an input label-led with x_i computes x_i , otherwise a node label-led with g_v computes $g_v(f_1, \ldots, f_p)$ where f_1, \ldots, f_p are the functions computed by its predecessors. We say that the circuit computes some extension of it.

Our main result is:

Theorem 1. Assume that $f : \{0, 1\}^n \to \{0, 1\}$ can be computed by a k-ary monotone real circuit of size s. Then f can be computed by a binary monotone real circuit of size $O(sn^{k-2})$. Moreover, increasing the size to $O(sn^{k-1})$, we can assume that the circuit uses only unary gates and binary additions.

Here, binary addition is a fan-in 2 gate that adds the two real numbers. In the rest of this section, we prove Theorem 1. The main ingredient, Theorem 4, is to show that a monotone function on a finite set $S \subseteq \mathbb{R}^k$ can be computed by a binary monotone real circuit of size $O(\log_2(|S|)^{k-2})$. To conclude Theorem 1, we then note that in a monotone real circuit computing $f : \{0, 1\}^n \to \{0, 1\}$, the intermediary gates can be restricted to domain of size at most 2^n . Theorem 4 itself is proved using two technical lemmas. Lemma 2 in its simplest, but already nontrivial, form states the following: a monotone two-valued function $f: S_0 \to \{0, 1\}$, with $S_0 \subseteq \mathbb{R}^2$ finite, can be computed using one binary addition and unary monotone gates. The lemma is then extended to talk about an arbitrary k, as well as about a finite union of two-valued functions, under the assumption that their domains and ranges are appropriately ordered. In Lemma 3, we take a monotone *k*-ary function f and "stretch" its domain so that Lemma 2 becomes applicable. This allows to compute *f* using functions of arity k-1 and proceed inductively.

Lemma 2. Let S_0, \ldots, S_m be finite subsets of \mathbb{R}^k , $k \ge 1$, such that $S_i \subseteq (i, i + 1)^k$ for every *i* and let $S := \bigcup_{i=0}^m S_i$. Assume that $f: S \to \mathbb{R}$ is a monotone function such that $f(S_i) \subseteq \{2i, 2i + 1\}$ for every *i*. Then there exist monotone functions *g*, *h* such that for all $\langle x_1, \ldots, x_k \rangle \in S$,

$$f(x_1,...,x_k) = g(x_1 + h(x_2,...,x_k))$$

Proof. We identify $\mathbb{R} \times \mathbb{R}^{k-1}$ with \mathbb{R}^k . Let $X_i := \{x \in \mathbb{R} : \exists y \in \mathbb{R}^{k-1}, \langle x, y \rangle \in S_i\}$ and $Y_i := \{y \in \mathbb{R}^{k-1} : \exists x \in \mathbb{R}, \langle x, y \rangle \in S_i\}$ be the projections of S_i to first coordinate, and the last k-1 coordinates, respectively. Let $Y := \bigcup_{i=0}^m Y_i$. For $y \in Y$, let

$$\begin{aligned} &\alpha(y) := \min\left(\{x \in X_i : f(x, y) = 2i + 1\} \cup \{i + 1\}\right) \,, \\ &\text{if } y \in Y_i. \end{aligned}$$

This guarantees that, for every $\langle x, y \rangle \in S_i$, f(x, y) = 2i + 1 iff $x \ge \alpha(y)$. Since $|x - \alpha(y)| < 1$, we can write

$$f(x, y) = \lfloor (2i + 1 + x - \alpha(y)) \rfloor$$
, for every $\langle x, y \rangle \in S_i$

Since *f* was a monotone function, $-\alpha$ is a monotone function on each of the sets *Y*_{*i*}. Define

$$h(y) := 2i + 1 - \alpha(y)$$
, if $y \in Y_i$.

The function is monotone on every set Y_i . Moreover, since $h(S_i) \subseteq [i, i + 1]$, h is monotone on the whole of Y. This gives the expression $f(x, y) = \lfloor x + h(y) \rfloor$ as required. \Box

Lemma 3. Let $f : S \to T$ be a monotone function where $S \subseteq \mathbb{R}^k$ and $T \subseteq \mathbb{R}$ are finite sets. Let $t := \lceil \log_2 |T| \rceil$. Then f can be computed by a monotone real circuit of size O(k(t - 1)) such that the circuit uses only unary gates, binary addition gates, and t gates of arity k - 1.

Proof. W.l.o.g., we can assume that $S \subseteq (0, 1)^k$ and $T = \{0, 1, ..., 2^t - 1\}$. The circuit is constructed by induction with respect to *t*. For t = 0, the function is constant. If t = 1, this is simply Lemma 2 (with m = 0). Assume that t > 1 and let $f' := \lfloor \frac{1}{2}f \rfloor$. Hence, $f' : S \to \{0, ..., 2^{t-1} - 1\}$ and assume we have constructed a circuit for f'. For $x = \langle x_1, ..., x_k \rangle$, define $i + x := \langle i + x_1, ..., i + x_k \rangle$, and let $S_i := \{i + x : x \in S\}$. Define $h : \bigcup_{i=0}^{2^{t-1}-1} S_i \to \{0, ..., 2^t - 1\}$ by putting, for $z \in S_i$ of the form z = i + x,

$$h(z) := 2i \qquad \text{if } f(x) \le 2i \\ 2i+1 \qquad \text{if } f(x) \ge 2i+1$$

The function is monotone on each of the sets S_i , and since $h(S_i) \subseteq \{2i, 2i+1\}$, it is monotone on the whole $\bigcup_{i=0}^{2^{i-1}-1} S_i$ The definition guarantees that, for all $x \in S$,

$$f(x) = h(f'(x) + x).$$
 (1)

By Lemma 2, h can be computed by a circuit with 3 non-input gates, such that the circuit uses one binary addition, one unary gate, and one gate of arity k - 1. Hence, by (1), f can be computed from f' using one additional (k-1)-ary gate and k+2 binary addition/unary gates. This gives the required circuit for f. \Box

¹ Also, the assumption $\sup\{|f(x)| : x \in S\} < \infty$ could be removed, had we decided to work over $\mathbb{R} \cup \{\pm \infty\}$.

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