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High-level synthesis of on-chip multiprocessor architectures based on answer set programming

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*Highlights (for review)

Highlights

- This paper presents a system-level synthesis methodology based on Answer Set Programming (ASP) for heterogeneous multiprocessor on chip.
- The proposed approach relies on a high-level description of an application (its timing constraints, available resources, and the physical restrictions of the target device) to produce the optimal computing infrastructure made of heterogeneous processors, peripherals, memories and communication components. Final multi-objective optimization aims at maximizing speed, while minimizing chip area.
- We addressed the problem of size explosion encountered in similar synthesis methodologies (such as Integer Linear Programming or Constraint Programming) by providing a new compact ASP encoding that is able to generate optimal solution while reducing considerably the overall synthesis runtime.