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Self-start-up fully integrated DC-DC step-up converter using body biasing technique for energy harvesting applications

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ABSTRACT

An ultra-low power, self-start-up switched-capacitor Two Branch Charge Pump (TBCP) circuit for low power, low voltage, and battery-less implantable applications is proposed. In order to make feasible the low voltage operation, the proposed charge pump along with Non-Overlapped Clock generator (NOC) are designed working in sub-threshold region by using body biasing technique. A four-stage TBCP circuit is implemented with both NMOS and PMOS transistors to provide a direct load flow. This leads to a significant drop in reverse charge sharing and switching loss and accordingly improves pumping efficiency. A post-layout simulation of designed four-stage TBCP has been performed by using an auxiliary body biasing technique. Consequently, a low start-up voltage of 300 mV with a pumping efficiency of 95% for 1 pF load capacitance is achieved. The output voltage can rise up-to 1.88 V within 40 µs with 0.2% output voltage ripple in case of using 400 mV power supply. The designed circuit is implemented by 180-nm standard CMOS technology with an effective chip area of 130.5 µm × 141.8 µm while the whole circuit consumes just 3.2 µW.

1. Introduction

Over the past few years, intensive research has been conducted on self-powered biomedical devices including implantable and wearable electronics. These devices are being utilized in different applications such as pacemakers, cochlear implants, etc. To obtain a long lasting performance, these devices are required to be powered by an external source. Supplying the device with sufficient energy over a long lifetime is one of the main challenges in biomedical implant systems. Using any kind of battery in such a device is not convenient; Small batteries need to be replaced frequently and large batteries increase the sensor size which is absolutely undesirable. Ideal implantable systems harvest energy from ambient sources such as thermal gradients, mechanical vibrations, and RF sources which potentially provide unlimited lifetime [1,36]. The obtained voltage is very low and has to be up-converted to be sufficient to supply the sensor. So the design of a low input voltage DC-DC up-converter, that can efficiently extract energy, is critical for self-powered systems.

Different start-up mechanisms are reported in the literature using auxiliary batteries [2,3], mechanical switches [4], and RF [5]. These all need additional off-chip components which limit the practical application of the system [2,4,6,17].

On the other hand, inductive and capacitive low voltage up-converters exist for charge transfer. The inductive approach uses various start-up techniques to kick start the system which reduces the minimum operation voltage and therefore has a higher efficiency [2,4]. However, the requirement of bulky components is the disadvantage of this approach [21]. The capacitive up-converters does not need any bulky components while having a lower efficiency.

This kind of DC-DC converters are known as Switched Capacitor (SC) power converters and they consist of power stage (also known as Charge Pump (CP)) which is an array of capacitors. The topology of the DC-DC step-up converter is shown in Fig. 1. The switched capacitor charge pump cascades charge pump stages.

The challenge in designing a CP for low voltage applications is the clock oscillator that can operate under low voltages. Ultra-low power sub-threshold ring oscillators are reported in [15,16]. Body biasing approaches are applied to operate CMOS inverters in the sub-threshold region that introduce performance improvement of the ring oscillator.

In this paper, a self-start-up fully-integrated DC-DC step-up converter is proposed. It consists of a charge pump and a non-overlap clock generator circuit.

A block diagram of the proposed structure is shown in Fig. 1. A symmetric cross-coupled TBCP is designed by using two CTSs and a compensating structure at each stage. Clk and $\overline{\text{Clk}}$ are two non-overlap clock signals that are generated by the NOC circuit. The proposed

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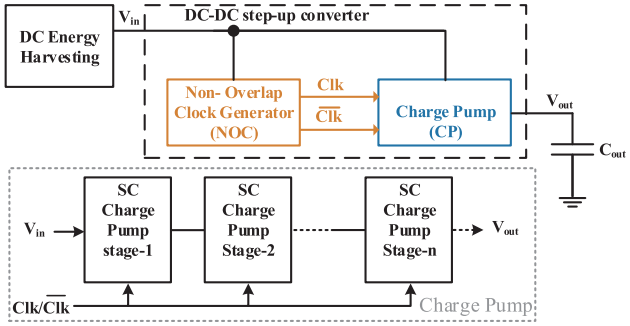

Fig. 1. The topology of the DC-DC step-up converter.

structure works in sub-threshold voltage range with no external start-up voltage requirement. The designed circuit can be used for low power battery-less implantable applications supplied with harvested energy. Working in low voltage range has the benefit of low dynamic power consumption while suffering from high power loss due to CMOS leakage. To minimize the CMOS leakage, body biasing technique is applied to the transistors in CP and NOC circuits. It adaptively tunes the body bias voltage of the transistors in such a way that the threshold voltage increases in idle mode and decreases during active periods. This is achieved by adjusting the bulk voltage of charge pump transistors using two auxiliary NMOS and PMOS transistors.

Conventional cross-coupled charge pump result in output voltage degradation as the transistors cannot turn on/off complementary in low voltage supplies. The proposed structure demonstrates advantages over the conventional structures, while working under low voltage supply:

- The proposed structure has a Symmetrical fully integrated design.
- Under low voltage supplies, body biasing technique can turn on/off the MOSFETs more effectively than TBCP.
- Body biasing technique is applied to MOSFETs to lower the threshold voltage which reduce the body leakage current.
- Two branches with both NMOS and PMOS reduce the reverse charge sharing loss.
- The proposed non overlap clock generator circuit with body biasing technique provides two out of phase clock signals under low voltage supply. This is an important part of this start-up charge pump design.
- Charge pump and NOC circuits work with same sub-threshold supply voltage.
- Improvement in Pumping efficiency, ramp-up time and output voltage ripple is achieved. Therefore, higher output charge transferability results in a faster output ramp-up time for a specified load capacitance.

The validation of the proposed structure is done by implementing conventional structures using TSMC 180-nm technology to quantify the benefits of the proposed structure.

The rest of the paper is organized as follows. Section 2 surveys the previous charge pump circuits. Section 3 includes the investigation on the body biasing techniques for cross-coupled voltage doubler. Section 4 describes the structure and operation of the proposed structure consist of four-stage TBCP along with two-phase non-overlapped clock generator. Section 5 presents the simulation results. Finally, conclusions are provided in Section 6.

2. Previous charge pump circuits

Most of the conventional CMOS charge pump used two out-of-phase signals to gradually accumulate and push the charge in each pumping capacitor in only one branch, such as Dickson CP [7]. The n-stage NMOS-based Dickson charge pump circuit is shown in Fig. 2.

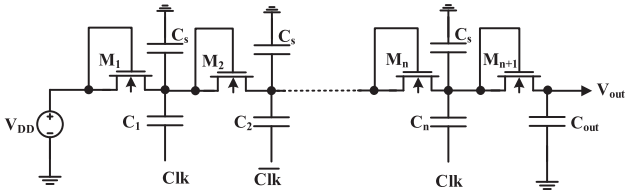

Fig. 2. N-stage Dickson charge pump [7].

The NMOS transistors operate as diodes so the voltage fluctuation (ΔV) at each pumping node must be larger than the threshold voltage of the MOSFETs,

$$\Delta V \geqslant V_{TH} \tag{1}$$

The voltage fluctuation at each pumping capacitors can be expressed as,

$$\Delta V = V_{clk} \times \frac{C_i}{C_i + C_s} - \frac{I_o}{f \cdot (C_i + C_s)} \tag{2}$$

where ΔV represents the single stage gain of one stage and explains the limited maximum output voltage caused by the increasing threshold voltage for body effect. V_{clk} is the voltage amplitude of the clock signals (same as the power supply), C_i and C_s are the pumping and parasitic capacitors respectively. I_o is the output current and f is the clock frequency. When the charge pump has to deliver a load current I_o, the output voltage is reduced by an amount that is inversely proportional to the switching frequency, f. If C_s and I_o are small enough and C_i is large enough, (2) can be simplified as,

$$\Delta V \approx V_{clk} = V_{DD} \tag{3}$$

Dickson CP suffers from threshold voltage drop across the drain-source terminal at each stage. Higher voltage drop happens at later pumping stages when the number of stages increases. In order to solve the problem of threshold voltage drop in Dickson CP, charge pumps with complicated structures have been developed [20]. One type of CP that use modified Charge Transfer Switches (CTSs) is an effective technique with two-phase clocking scheme [8], which gives better pumping voltage gain than the one in Dickson CP. As the charge is pushed into one branch of CTS, redistribution loss is not negligible between last stage and the output capacitor. If the voltage is too low, it may not be sufficient to turn on the transistors [12,13,22].

In [9] a linear CP (LCP) is proposed which is a modified version of [8], shown in Fig. 3. PMOS CTSs along with a systematic way to control the gate of PMOSs is used in this design to achieve high pumping efficiency. Each of the PMOS CTSs is controlled by a CMOS inverter by MN_i and MP_i. To avoid the body effect, the bulks of all CMOS transistors are connected to their sources. This design needs an additional stage and gate control strategy which is different in its first and last stages. It also cannot be turned on/off the transistors effectively if V_{DD} is less than the threshold voltage.

The design in [10] proposed two branches cross-coupled charge pump with two CTS branches including a compensator structure at each stage, as shown in Fig. 4. The gate control signals in two branches are intertwined. Two branches function as two individual CP circuit and their connected output drive a capacitive load. In this design, the pumping efficiency is improved and the output ripples are decreased since the charge transfer of the two branches has been improved. In comparison with the previous design, this structure is symmetric but it

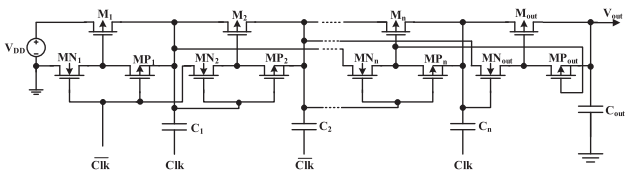

Fig. 3. N-stage linear charge pump circuit (LCP) [9].