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Review

InP high electron mobility transistors for submillimetre wave and terahertz frequency applications: A review

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ABSTRACT

This paper reviews the rapid advancements being made in the development of high electron mobility transistors (HEMTs) on InP substrates for future sub-millimetre wave (30–300 GHz) and terahertz (300 GHz to 3.5 THz) frequency applications. The InP HEMTs exhibits outstanding 2-DEG properties in InAlAs/InGaAs heterostructure. This paper highlights the rapid growths in the developments of enhancement mode (E-Mode) and depletion mode (D-Mode) InP HEMTs over the last 40 years, the use of InP HEMTs for cryogenic applications, reliability issues and kink effects in InP HEMTs in detail and it also highlights the impact of geometrical dimensions and their scaling on the performance of InP HEMTs. Their uniqueness in terms of low noise, low power dissipation, high gain and high frequency of operation has fuelled the incorporation of InP HEMTs in a wide variety of applications such as high speed wireless and optical communication systems, sub-millimetre wave (S-MMW) and THz receivers and transmitters, radio astronomy and radiometry, flight communications and sensing applications, material spectroscopy, active and passive imaging applications, biomedical instrumentation applications and high speed ICs such as low noise amplifiers (LNAs), multiplier chains, switches, multiplexers and flip-flops.

1. Introduction

The demand for sub-millimetre wave and terahertz monolithic integrated circuits (S-MMICs and TMICs) are increasing day by day in the semiconductor market due to their growing demands in applications such as internet and information technology, broadband and low noise wireless and optical communication systems, cell phones, satellite communication systems, material spectroscopy, radio astronomy and radiometry, receivers in atmospheric sensing, active and passive THz imaging applications, low noise amplifiers (LNAs) in phased array radars, multiplier chains, flight communications and sensor applications, preamplifiers and driver amplifiers, biomedical instrumentation applications, military, aero and space applications and also for other high speed ICs such as multiplexers and demultiplexers, oscillators for high resolution imaging, switches for broad band communication applications, frequency multipliers, flip-flops and mixers for transceiver up converter applications [1–31]. InP HEMTs have been considered as one of the most suitable transistor technologies for realizing the key components such as sub-millimetre wave (S-MMW) and THz receivers and transmitters [32–34], multiplexers/demultiplexers [35–50], low noise amplifiers (LNAs) [51–69], switches [70–73], Pre-amplifiers and driver amplifiers [74,75], Flip-flops [76–78], Power amplifiers [79–84], oscillators [85,86] and Frequency multipliers and up-converters [87–90] required for future THz wireless and optical communication systems.

Over the last 50 years, the speeds of transistors and ICs have been increased among which InP HEMTs have been demonstrated the highest f_T over 700 GHz and f_{max} over 1.5 THz. Several research groups have demonstrated amplification in InP HEMT based ICs which crosses 270 GHz [54], 308 GHz [62], 480 GHz [52], 670 GHz [68], 850 GHz [69], and 1THz [91]. This was made possible due to the tremendous improvement in the f_T and f_{max} of InP HEMTs by a combination of techniques such as reducing gate length, increasing indium content in the quantum well (QW), by adopting δ-doping technique and source/drain/gate/channel engineering [91–109]. The advancements in band gap engineering and the rapid growth in the development of thin film deposition techniques such as MBE and MOCVD results in the successful development of HEMTs. The first HEMT was experimentally demonstrated by T. Mimura and his team of researchers from Fujitsu Lab,

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Table 1
Comparison of DC and RF performances of some of the popular InP HEMTs (D: Depletion Mode, E: Enhancement Mode, Ref: Reference).

Ref.	Gate Length L_g (nm)	Mode	f_T (GHz)	F_{max} (GHz)	g_m (mS/mm)	I_{DS_max} (mA/mm)
[144]	300	E	116	229	701	≈400
[203]	120	D	166	340	1100	800
[98]	100	D	305	340	1550	≈500
[135]	100	D	249	415	1051	724
[143]	100	E	208	460	912	≈400
[205]	80	D	310	330	2630	700
[140]	75	D	270	910	2190	800
[134]	60	D	710	478	2114	≈650
[150]	60	E	169	–	544	225
[202]	50	D	496	400	2000	≈1200
[204]	50	D	490	–	1900	1400
[149]	50	E	465	1060	1750	≈750
[139]	50	D	557	718	≈1650	≈700
[136]	40	D	491	402	2000	≈800
[210]	30	D	547	400	1500	≈1000
[128]	30	D	644	681	1900	≈850
[139]	30	D	628	331	1620	≈750
[151]	30	E	601	609	1830	≈680
[206]	30	D	368	368	918	≈600
[91]	25	D	610	1500	3100	≈1180
[131]	25	D	562	330	1230	800

Japan at 1980 [110]. The HEMT was developed based on modulation doping process in III-V hetero-structures which was first successfully illustrated by Ray Dingle and team from Bell Lab, USA at 1978 [111]. Aksun et al [112] reported the first InP HEMT performance in 1986 which has an $In_{0.53}Ga_{0.47}As$ channel grown on a lattice matched InP substrate. In recent years, significant advancements have been reported in the growth of InP wafers in terms of its wafer size (4 in. and 6 in.) with good mechanical strength. The large wafer size is highly desirable for semiconductor industry in order to reduce the production cost which was the earlier drawback of InP HEMTs. Lai et al. [18] reported an f_{max} of over 1THz for the first time using 50 nm InP HEMT technology in 2007. Later Mei et al. [91] improved the f_{max} to 1.5 THz using 25 nm InP HEMT process. Table 1 shows the f_T and f_{max} reported for some of the popular InP HEMTs.

2. Developments in D-MODE InP HEMTs

From Table 1, it is clear that the D-Mode InP HEMTs are superior in DC and RF performances when compared with E-Mode InP HEMTs. The highest g_m reported for D-Mode InP HEMT is 3100 mS/mm which was reported by Mei et al. in 2015 using 25 nm InP HEMT process and that 25 nm InP HEMT also holds the record for highest f_{max} of 1500 GHz for any InP HEMTs [91]. Xiaobing Mei et al. in 2015 demonstrated the first ever THz LNA MMIC using 25 nm D-Mode InP HEMT process. Chang et al. reported the highest f_T of 710 GHz for any InP HEMTs using 60 nm InAs channel based D-Mode InP HEMT process [134]. The most important factors which significantly affects the DC and RF performances of InP HEMTs are scaling of gate length, Indium concentration in the channel, spacing between source and drain, thickness of the InAlAs barrier (t_{ins}), thickness of the channel layer (d_c) and side recess spacing (L_{side}) [113–139]. From the literature, it is found that increasing the InAs concentration in the channel and reducing the spacing between source and drain is essential for achieving THz frequency of operation [113–139].

This section covers the impact of gate length scaling, channel layer thickness scaling, barrier layer thickness scaling and the side recess spacing scaling on the DC and RF performance parameters of D-Mode InP HEMTs in detail. Dan et al. [135] demonstrated that the increase of the space between gate and drain regions are highly desirable for obtaining higher breakdown voltage for InP HEMTs. Increasing the spacing between gate and drain can effectively reduce the avalanche multiplication of electrons by relaxing the strength of electric field [135]. Therefore Asymmetric gate recess structure is highly desirable for high power applications because this structure can effectively enhance the breakdown voltage of the devices by relaxing electric field strength of the gate-drain regions [140,141]. There is no doubt that D-Mode InP HEMTs have been considered as outstanding solid state transistor technology for next generation THz frequency applications including 4G/5G communications due to their superior RF performance in comparison with E-Mode InP HEMTs and HEMTs on any other material systems.

Kim et al. [129] and his fellow researchers at Microsystems Technology Laboratories (MTL), Massachusetts Institute of Technology

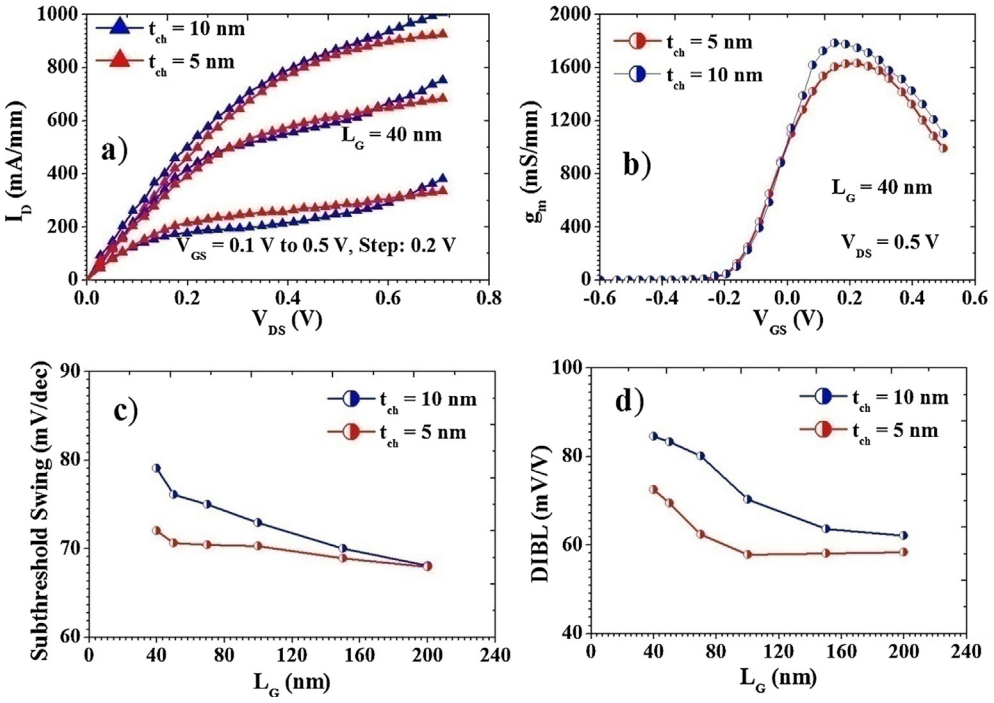

Fig. 1. (a) The impact of channel layer scaling on the output characteristics of L_G = 40 nm D-Mode InP HEMT. (b) The impact of channel layer scaling on the transconductance (g_m) characteristics of L_G = 40 nm D-Mode InP HEMT. (c) The impact of channel layer and gate length scaling on the subthreshold swing (SS) of the D-Mode InP HEMT and (d) the impact of channel layer and gate length scaling on the drain induced barrier lowering (DIBL) of the D-Mode InP HEMT [129].