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Fault tolerant adaptive write schemes for improving endurance and reliability of memristor memories

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ABSTRACT

The non-deterministic nature of memristor and its unreliable behavior are the two major concerns hampering its growth and industrial manufacturability. The endurance and reliability of memristor memories are affected not only by the process variations (intrinsic), but also due to the electrical stress created by interfacing peripheral circuits (extrinsic). Concerning the intrinsic faults in transition metal oxide (TMO) memristors, drifting of oxygen vacancies across the device is responsible for SET/RESET operation. It is likely that such drifting might induce switching faults during the device operation, for instance endurance of the memory. Thus, the application of a fixed write pulse may not suffice to achieve successful write operations under these circumstances. To circumvent the above pitfall, we propose here a new technique by designing a fault tolerant adaptable write scheme which can adapt by itself based on the behavior and switching faults. Accordingly, the proposed write scheme identifies the optimal amplitude and the width for write pulse. The proposed write scheme under various memristor faults is found to enhancing the reliability of memristors efficiently. Further, the results are validated by means of Monte-Carlo analysis by infusing the random variations of internal parameters of memristors as well.

1. Introduction

Semiconductor industries, as well as researchers, face unprecedented challenges to the niche issues centered on scaling of technology both functionally and dimensionally. Considering the present day memory technologies (SRAM, DRAM, and flash) are facing utmost challenges regarding its size, leakage power, and speed [1–4]. Therefore, there is an immediate need to find efficient yet reliable memory technology which should be compatible with CMOS process, but it should necessarily allow further scaling, non-volatile storage, low power consumption, high speed of operation and improved performance. Resistive Random Access Memory (RRAM), Phase Change RAM (PC-RAM), Ferroelectric Random Access Memory (FRAM) and Spin-Torque Transfer RAM (STT-RAM) are regarded as emerging class of non-volatile memory technologies and potential replacement for SRAM, DRAM and Flash memories. Among the next-generation memory technologies, MRAM and FRAM face the dimensional scaling issues something similar to the present technologies [5–6]. Amongst these, PC-RAM consumes more power to change the phases between the crystalline and amorphous states [7] But, RRAM [1–2,8] appears to be the excellent choice because it can be miniaturized below 10 nm. Nevertheless, it must overcome the integration, reliability and performance challenges before being considered as next generation memory device. Many industries namely HP, Samsung Electronics, Sharp, Fujitsu, Unity Semiconductor Corp, Hynix and Adesto Technology Inc. and Micron Technology are working on memristor based RRAM technology [9–10]. Since the memristors are not available commercially, the researchers are trying to design memristor emulators [11–13] to develop the memristor circuit applications [14–15]. Memristor is a type of resistive random access memory realized theoretically by Leon Chua in 1971 [16] and implemented physically by HP labs in 2008 [17]. It is regarded as a two terminal passive device which links the missing link between flux (ϕ) and charge (q) connecting the fourth missing fundamental circuit element. Memristor can be used for numerous applications such as digital logic [18–19],neuromorphic systems [20–22], analog circuits [14–15,23–24], image processing [23–24], and memory [25–26]. MIM (Metal-Insulator-Metal) is one of the proven structures to fabricate memristors due to their excellent yet reproducible resistive switching behaviors. The resistance of the insulating layer sandwiched between two metal layers varies with respect to the magnitude, polarity and width of the electric bias applied to it. Most importantly the device remembers its most recent value of the resistance when the bias is turned off. Thus by changing the resistance state of the insulator between a low resistance state (LRS) and a high resistance state (HRS), the

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device can be manipulated to store logic 1 or logic 0 respectively by virtue of its different verified mechanisms such as conducting filament formation in both organic and inorganic materials, or conductivity change due to the redistribution of anions and cations [27]. Interestingly enough, by increasing the number of resistance states, one memory cell can store multiple bits (Multilevel Cell) [25,28].

Switching from HRS to LRS is called as SET operation, whereas the change-over from LRS to HRS is called RESET operation. Most of the memristor based memory designs assume SET state as logic 1 (ON state) and RESET state as logic 0 (OFF state). Memristor memory cells can be classified into bipolar device, and unipolar device based on the polarity of the applied voltage for SET and RESET operations. A unipolar device requires single polarity voltage to store logic 1 or logic 0 while bipolar device needs opposite polarities to store logic states.

One of the simplest methods to design a memristor memory is to construct crossbar architecture with memristor cell placed at the crossing points of the rows and columns. This arrangement is termed as 1 M (one Memristor) memory, and it offers the highest density roughly as $4F^2$ (F is termed as feature size) [29–30]. One of the prominent challenges to access an individual cell in crossbar arrays is to manage the sneak path problem [31–33] that leads to operational failure and high power consumption.

When we apply voltage/current to access the particular cell, the sneak paths are formed, and voltage/current is being supplied to the unselected devices as well. This creates unnecessary disturbances to the content of unselected cells. Several methods were suggested to solve the sneak path issues [33–34]. The basic idea to diminish the sneak path disturbance is to use rectifying device or selector device such as diode or transistor to select the cell. Hence this method requires placement of one selector device and one memristor at each junction of the crossbar array. The crossbar architecture can be stacked on CMOS peripherals to design the three dimensional (3D) ICs.

Reliability of the memristor memories are mainly affected by data retention, endurance, random telegraph noise, write disturbance, read disturbance, sneak path issues, crossbar array defects, and radiation effects [35–40]. TMO (Transition Metal Oxides)based bipolar memristor device shows excellent endurance characteristics than other type of memristor devices [5,8]. Table 1 provides the strength and length of the write pulses to SET and RESET the single cell TMO based bipolar memristor devices [41–49]. From the Table 1, it is clear that most of the memristor materials behave asymmetrically for both polarities of the write voltages. So, the write drivers should be capable of supplying appropriate bias to perform the successful SET/RESET operations.

Although the TMO based device exhibits potential endurance characteristics, they suffer from uncontrolled filamentary switching defects which result in reduced endurance cycles [50–51]. In the TMO based memristors, the SET and RESET operations are achieved by drifting the oxygen vacancies ($V_{OX}{}^{+2}$) back and forth. But it is essential to drift the same quantity of vacancies back and forth for each SET and RESET operations to perform the successful write (logic 1/logic 0) operations [37]. But practically, it is apparent that drifting the oxygen vacancies equally is challenging. It is likely that such drifting might induce switching faults during the device operation. As a result, these induced faults affect the endurance performance of the memory. Since the memristor device shows considerable variations within the same material, the fixed write voltages may not work efficiently to achieve successful write operations for all the memory chips. So, it is required to tune the amplitude and width of the write pulses for proper SET and RESET actions [37,52]. As a matter of fact, a few research papers [53–57] elucidate to detect SET/RESET(LRS/HRS) faults by enabling built-in self-test and to facilitate the repair by invoking a built-in self-repair. Nevertheless, this research paper presents a methodology to prevent such faults. The paper evidently discusses the following approach and the outcome thereof,

(i) Identification of defects and faults responsible for reliability and endurance of the memory.
(ii) Fault injection and simulation for the potential defects that reduce the endurance cycles.
(iii) Adaptive tuning mechanisms to determine the optimum pulse amplitude and width to store logic 1 and logic 0.
(iv) Monte Carlo simulations to prove that the proposed technique works efficiently.

Based on the above approaches, we propose here a new approach by designing a fault tolerant adaptable write scheme which can adapt by itself based on the behavior and faults of the memristor. The proposed write scheme identifies the optimal voltage amplitude and duration for write operations. The results are validated by means of Monte-Carlo analysis by infusing the random variations of memristor internal parameters viz., R_{on} and R_{off}. As such, the simulation results affirm that such random variations in write scheme under various memristor faults (both intrinsic and extrinsic) found to enhancing the reliability of memristors efficiently.

2. Memristor memory: operation and faults

2.1. Memristor cell

Memristor cells are fabricated by using transition metal oxide (TMO) materials like titanium dioxide (TiO_2), zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2), zinc oxide (ZnO) and tantalum oxide (TaO), etc [41–44]. Fig. 1a) shows the general structure of TMO based memristors. It consists of metal oxide thin film (semiconductor) placed between two metals. The length of the metal oxide thin film is D, and it has two regions namely oxygen vacancies filled doped region of width w and highly resistive undoped region of width D-w. Fig. 1b) shows the electrical equivalent model of the memristor and Fig. 1c) is the symbol of the memristor.

When the positive terminal of the memristor is connected with a positive voltage and the negative terminal of the memristor is connected to ground, the dopants move towards the undoped region hence increases the conductivity of the memristor. On the other hand, when a negative voltage is applied, the dopants move towards the doped region; thereby increases the memristance of the device. When the supply voltage is disconnected, the dopants rest at their present position; thus, remembers the last value of the resistance. This property of the memristor is used to design the nonvolatile memory circuits. Reading the

Table 1
Write pulse variations in different TMO memristor.

Memristor type	Write-1 voltage (V)	Write-1 pulse width	Write-0 voltage (V)	Write-0 pulse width	Endurance cycles
SEMATECH-HfO_x [41]	1.5	50 ns	−1.5	50 ns	10^9
Panasonic-TaO [42]	1.5	100 ns	−2	100 ns	10^9
IMEC-HfO_2/Hf,Ti [43–44]	1.8	5 ns	−1.8	10 ns	10^{10}
HP-TaO [45]	1.9	1us	−2.2	1.5u	1.5×10^{10}
ITRI-HfO_2/Ti [46–47]	3.2	40 ns	−2.7	40 ns	10^{10}
SAIT-TaO [48–49]	4.5	10 ns	−7	10 ns	10^{12}