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A variation tolerant current mode low swing signaling approach for gigascale on-chip interface circuit

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ABSTRACT

Enhanced functionality per unit area is the gradually increasing demand of current manufacturing market and that desire has been fulfilled by aggressive down scaling of technology, which has adversely influenced the delay of global interconnect thereby affecting the performance of high speed design. As the time needed to charge or discharge the output node of a circuit is directly proportional to the peak-to-peak swing of the driven signal, there remains an inherent speed advantage in low swing signaling, which is considered to be one of the most suitable options to eliminate signal integrity issues in multi-gbps chip-to-chip communication. This article unveils a detailed report on the shortcomings of existing low swing signaling schemes, where no work is witnessed to generate a certain low voltage swing across any reference voltage ranging from 'Logic 0' to 'Logic 1' of the input signal. To address the same, we have come up with a novel methodology consisting of two different current sources (one at driver and the other at receiver) made of NMOS. In this case, the said reference voltage corresponds to the threshold of the receiver chip, which has to be identified at first. The simulation of proposed low swing signaling scheme is carried out using 65 nm, 45 nm and 22 nm CMOS technology to examine the performance metrics at 1.1 V supply while switching at 2 GHz. This approach does provide extensive delay and energy or PDP savings to outsmart the existing works.

1. Introduction

With the continuous advancement of technology, the die size of a chip becomes smaller and compact, which in turn affects the delay of the channel between driver and receiver thereby affecting the performing ability of high speed digital system. This restricts the data rate between any two communicating chips of a server to increase radically [1]. While driven at GHz range, the largely dense lossy interconnect in PCB and packages encounters major signal integrity issues because of dispersion (engendered by dielectric fluctuations with angular frequency), reflection (S_{11}) and insertion losses (S_{12}) of channel made of copper [2,3]. When a pulse (width = τ and amplitude = V_0) is steered to move through a lossy channel, the width gets widened due to dispersion and the amplitude reduces due to the effect of S_{12} and S_{11}. The rise in pulse width at different parts of the channel signifies to experience different skin effect and dielectric loss resulting in different effective resistances. This impedance mismatch leads to reflection noise which makes the detection of received signal difficult. Therefore, a channel with limited bandwidth is the major restricting factor to the comprehensive performing ability of an electronic system with data sampling rate above 10Gbit/sec [4–6]. Advancement in semiconductor technology towards ultra-deep submicron regime has resulted in manufacturing of smaller chip and faster switching devices [7]. Market demand of improved functionality per unit area is fulfilled up to a certain range through extensive technology scaling, which has a great adverse effect on global on-chip interconnect delay thereby cutting down the system performance. This scaling has made the on-chip signal to be travelled across the longer interconnect by reducing the delay budgets [8,9]. Longer interconnects lead to more energy consumption as the length of interconnect is proportional to the capacitive effect. It is seen from [10] that, 40% of the total energy consumption is for the interconnect wires rather than associated drivers or receivers. Also, the signal integrity issues of such wires come into the picture in nano-meter regime as coupling between the neighboring lines causes crosstalk leading to the distortion of original switching waveform [11]. To get rid of such problems, circuit designers have already started to think of different methodologies like repeater insertion [12], low swing signaling [13–16] and bit encoding [17,18] to consider a trade-off between power and delay. The low swing technique is considered to be one of the best, as it depends on the dynamic energy of the low swing

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voltage. If the voltage swing gets reduced in a data path circuit, it leads to the smaller charging and discharging of the wire capacitance than that of in the case of full swing signaling [19]. As a result, the on-chip communication becomes more faster and energy efficient. Moreover, when the on-chip interconnect length and its fan-out cannot be reduced, this low swing technique is the best suitable method to obtain power and energy efficient on-chip circuits.

The rest part of the paper is organized as follows: The novel contribution of this article is stated in Section 2. Section 3 gives a clear overview and qualitative analysis of the existing low swing architectures. In Section 4, we have presented the proposed low swing generation scheme along with its working principle and mathematical modeling. The performance metrics of the proposed circuit are highlighted in Section 5, thereby claiming why it is to be chosen ahead of the existing schemes. In Section 6, the proposed model is tested on a receiver chip consisting of static inverter to generate full swing inside the chip and issues around it. Section 7 solves those issues by incorporating a novel circuit arrangement using dynamic CMOS inside receiver chip. The final circuit is also tested with arbitrary input data stream and is presented in Section 8. Finally, Section 9 concludes the work.

2. Novel contributions of the paper

In this work, we have reported a novel current mode low swing signaling scheme made of two different current sources to generate a certain low voltage swing at the receiver's end to replicate the attenuated received signal passed through an unmatched channel, while driven at multi-Gbps data rate. The main feature of this scheme is that, a certain low voltage swing can be originated across any reference voltage, which ranges from the 'Logic 0' to 'Logic 1' level of the driven input voltage. The block diagram of the proposed signaling scheme is shown in Fig. 1.

The NMOS at the driver pumps up current to the channel depending on the input logic it has. Also, the current flows through it is set by varying the width of that NMOS to obtain the higher voltage level (V_{MAX}) of a certain swing at receiver. The receiver uses a constant current source, which mainly shifts the voltage level of the attenuated received signal and defines the lower voltage level (V_{MIN}) of the swing generated. In this case, a self-biased NMOS serves as constant current source. Both the ends of the transmission line are terminated with a resistance of 50Ω (Characteristic Impedance) so as to have no reflection. When the input of NMOS at driver is steered by a 'Logic 1', it pumps current and a portion of that current is passed through the channel thereby increasing the voltage level up to V_{MAX} at the receiver. When the driver NMOS is fed by a 'Logic 0', it gets turned OFF thereby passing no current through the channel to drop the voltage at receiver end at V_{MIN}. Though there are numerous advantages of current mode signaling such as lower power consumption at higher frequency, low crosstalk and switching noise, less affected by voltage fluctuations and schematic simplicity, the biggest threat in this proposed scheme is to design an efficient sensing circuit to detect the voltage variation due to the change in current through the channel. From the above discussion, it is clear that the first step of proposed signaling methodology is to set

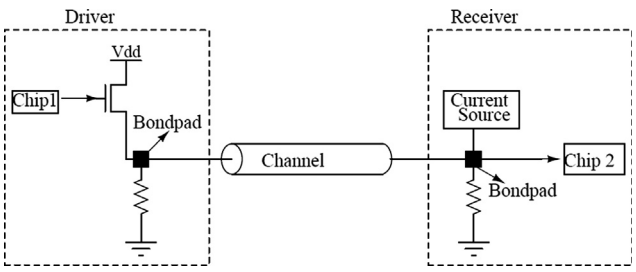

Fig. 1. Block diagram of the proposed low swing signaling scheme.

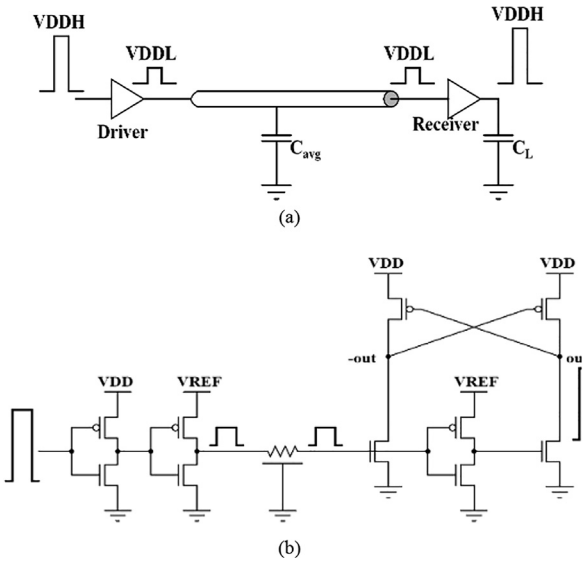

Fig. 2. Low swing signaling (a) typical low swing (b) schematic of CLC.

or define the threshold voltage (V_T) of the receiver. This V_T will correspond as the reference voltage across which, a certain low voltage swing is to be generated. In this work, we have considered to have a static CMOS inverter inside the receiver chip. The threshold voltage of that inverter is determined from voltage transfer characteristic (VTC). At last, a new circuitry incorporating dynamic CMOS inverter is used to replace the static one inside the receiver chip to obtain full voltage swing by reducing the extensive short circuit current which was flowing when static inverter was used. This approach eliminates the need of modifying the receiver design for effective detection of low swing signal. The simulation set up illustrates the effectiveness of the proposed current mode signaling while operated at 2 GHz switching frequency.

3. Prior research on low swing signaling

Although there are many different techniques to improve interconnect delay and crosstalk, they become less effective with the increase in switching speed. Low swing generation circuit carries the immense potential to improve such signal integrity issues for high speed applications. A typical low swing interconnect scheme is shown in Fig. 2(a). It consists of a driver, which converts the full-swing signal to a low swing before its propagation through interconnect and a receiver, which restores the low-swing signal to a full swing. The conventional low swing circuit (also known as Conventional Level Converter (CLC)) shown in Fig. 2(b) utilizes a PMOS feedback transistor. It outputs a signal swinging from 0 to V_{REF}. Though it is a noise immune circuit, the presence of additional propagation delay and high short circuit power dissipation, degrades its performance [20]. Thus different circuits are designed to obtain low swing interconnect so as to ensure energy and delay efficiency.

In [21], the CLC is modified using auxiliary cross coupled structure, which reduces delay time and eliminates the short circuit current during transition. Another low swing circuit using static driver and receiver and employing bootstrapping technique at the receiver side is depicted in [22], which requires low supply voltage and enhances the driving capability by reducing its delay time. But the requirement of extra capacitor in its design degrades its performance at high frequency. Reduced signal swing was also introduced with simple diode based drivers using diode connected transistor without the need of extra power supply and any multi-threshold process [23]. But due to its sensitivity to power supply variations, device parameters and loading conditions, its driving capability deteriorates for large loads. Symmetric

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