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A compact current-mode instrumentation amplifier for general-purpose sensor interfaces

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ABSTRACT

The proposed amplifier architecture follows a consolidated topology based on second-generation current conveyors (CCIIs), optimized for fully-differential operation. The architecture uses gain-boosting to improve the offset and noise characteristics of a recently proposed design. Wide input and output ranges and high accuracy are obtained by designing the CCIIs according to an original two-stage architecture with local voltage feedback. Embedding of chopper switch matrices into the amplifier enables vector analysis of the input signal, expanding the application field. The main strengths of the proposed amplifier are compactness and versatility. Measurements performed on a prototype designed with a 0.18 μm CMOS process are described.

1. Introduction

The instrumentation amplifier (in-amp) is the optimal choice for interfacing sensors that generate, either directly or indirectly, a voltage. An in-amp designed for general-purpose sensor interfacing should be able to amplify and demodulate sinusoidal signals, enabling complex impedance measurements or implementation of the lock-in approach [1]. At the same time, the in-amp should be configurable as a chopper amplifier to read dc signal with great accuracy [2]. In order to obtain compatibility with an as large as possible variety of sensors, a general-purpose in-amp should also have wide input common mode range (ICMR) and programmable gain. A unity gain option should be available to read sensors that produce relatively large output voltages, such as electrochemical gas sensors. Finally, compactness is mandatory to enable integration in low-cost systems on a chip (SoCs).

The classical three-op-amp [3] architecture generally does not meet the above criteria, since its first stage amplifies the differential mode while leaving the common mode unchanged, making the amplifier prone to saturation when the common mode is close to the rails. This architecture is also not optimized in terms of compactness and requires resistor trimming. Indirect current feedback amplifiers [4–6], involving direct application of the input differential signal to a differential pair, are less suitable to achieve the wide input ranges required in unity-gain settings. The current-balance in-amp uses source followers in the input stage [7] or even involves stacking of the input and output section [8], with severe limitation on the input common mode range and/or the output swing.

In this work, we propose a compact instrumentation amplifier based on second generation current conveyors (CCIIs) [9–10]. While the general architecture follows a well-known current-mode approach, the amplifier embodies also voltage-mode characteristics. A first example of the proposed architecture was presented in Ref. [11]. However, noise and offset performances of that preliminary version were not adequate for use in high accuracy sensor interfaces. In particular, flicker noise started to appear below 10 Hz, while statistical tests performed after Ref. [11] publication yielded input offset voltages up to 200 μV. Significant improvements of the offset and flicker noise characteristics have been obtained in the amplifier proposed in this paper by introducing gain boosting in the output stage. The effectiveness of the approach is demonstrated by means of experiments performed on a prototype designed with a 0.18 μm CMOS process. Measurements described in this paper include also tests that were not presented in Ref [11], such as statistical characterization of the offset voltage and quantitative estimation of the phase and magnitude errors achieved in demodulation experiments.

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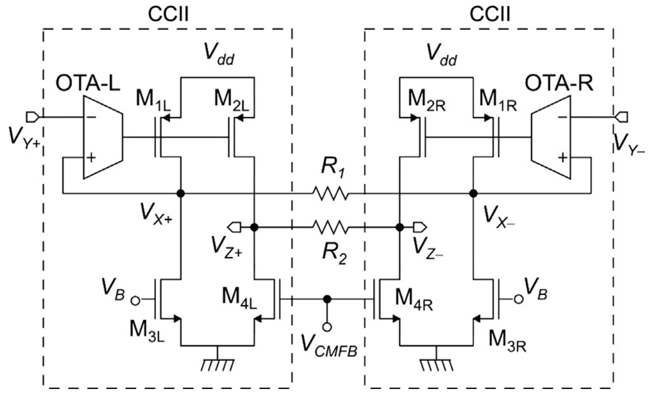

Fig. 1. Simplified view of the proposed instrumentation amplifier.

2. Circuit description

2.1. Principle of operation

A simplified schematic view that represents the principle of operation of the proposed architecture is shown in Fig. 1. Two identical CCIIs, indicated with dashed boxes in the figure, are connected to form a fully differential amplifier according to a scheme derived from Refs. [12,13]. Briefly, input voltages V_{Y+} and V_{Y-} are copied to nodes V_{X+} and V_{X-}, respectively. Thus, a current $(V_{IN+}$-$V_{IN-})/R_1$ flows across resistor R_1 and is replicated as a differential current across nodes V_{Z+} and V_{Z-}, so that R_1 and R_2 carry the same current. It can be easily shown that the differential-to-differential gain is given by:

$$A_{dd} = \frac{R_2}{R_1} \tag{1}$$

Let us consider the CCII on the left, since the same considerations applies to the right section. Note that M_{1L} forms a common-source inverting amplifier biased by a constant current provided by M_{3L} (V_B is a constant voltage). The cascade of the M_{1L}-M_{3L} amplifier and the single-stage amplifier indicated with OTA-L forms a two stage operational amplifier (op-amp) that, thanks to the voltage feedback connection, transfers voltage V_{Y+} to V_{X+}. Since M_{2L} is nominally identical to M_{1L}, current I_{D2L} tracks I_{D1L}.

For symmetry reasons, in nominal conditions, $I_{D3L} = I_{D4L}$, thus the currents exiting terminals V_{X+} and V_{Z+} are identical, as required by the CCII definition. The desired output common mode voltage is set by varying I_{D4L} and I_{D4R} through V_{CMFB}, controlled by a conventional common mode feedback (CMFB) loop. The input amplifiers OTA-L and OTA-R are designed to provide a rail-to-rail ICMR. In these conditions, the input common mode range of the whole amplifier is limited only by the maximum swing of voltage V_X, as shown in next section.

2.2. Proposed in-amp architecture with embedded chopper modulators

Blocks S_{IN} and S_{OUT} in Fig. 2 are chopper modulators, consisting in switch matrices that, depending on the logic value of the clock, transmit the signal along either the solid or dashed paths indicated inside the S_{IN}-S_{OUT} symbol, and labeled with the clock value ("0" or "1") that enables them. For simplicity, arrows and labels inside the chopper modulator symbols will be omitted in the rest of the paper. Demodulation is performed by S_{OUT}, controlled by clock *ck*. If the input signal does not require modulation, then $ck_{chop} = 1$, and S_{IN} becomes transparent. Otherwise, setting $ck_{chop} = ck$ enables chopper modulation. Block CA is a unity-gain current amplifier, the purpose of which is lowering the resistance seen by modulator S_{OUT}, greatly increasing the frequency response. Capacitors C_{O1} and C_{O2} are added to operate pre-filtering of demodulation byproducts.

Application of the modulation/demodulation scheme of Fig. 2 to the amplifier of Fig. 1 leads to the circuit of Fig. 3, representing the proposed amplifier. The current amplifier CA consists of the common-gate stage M_{22L}-M_{22R}, which forms a cascode structure with M_{2L} and M_{2R}. In order to equalize M_{1L} and M_{2L} drain-source voltages and improve precision of the $I_Z = I_X$ relationship, common gates (M_{11L}, M_{11R}) are also introduced in the "X" section of the CCIIs. The same cascode structure is applied to the lower part of the circuit, composed of n-type devices. Modulator S_{OUT} is split into S_1 and S_2: the former actually implements signal (I_{2L}-I_{2R}) demodulation, whereas the latter is necessary to modulate the offset and flicker noise components of bias currents I_{D4L} and I_{D4R}.

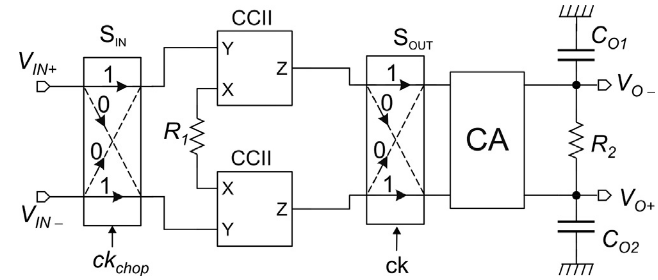

Fig. 2. Demodulation scheme. CA is a current amplifier. For demodulation functions, only clock *ck* is active. To implement chopper modulation, ck_{chop} is set equal to *ck*.

To reduce offset and low frequency noise contributions from $M_{22L\text{-}R}$ and $M_{44L\text{-}R}$, which do not benefit from the modulation effect of S_1 and S_2, these devices have been included into individual feedback loops, based on amplifiers $A_{NL\text{-}R}$ and $A_{PL\text{-}R}$, respectively, forming a gain-boosting configuration [14]. Offset and noise from $A_{NL\text{-}R}$ and $A_{PL\text{-}R}$ is rejected by the combined action of S_1 and S_3, for $A_{NL\text{-}R}$, and S_2, S_4 for $A_{PL\text{-}R}$.

Resistors $R_{1L} = R_{1H}$ and $R_{2L} = R_{2H}$ are such that $R_{1L} + R_{1H} = R_1$ and $R_{2L} + R_{2H} = R_2$. Groups R_C,C_C implement standard Miller compensation of the mentioned two–stage feedback loop. Constant voltages V_{B2} and V_{B3} are generated by conventional bias circuits.

Dummy switches S_{DP} and S_{DN} (always on) are introduced to compensate for the static voltage drop introduced by modulators S_1 and S_2, respectively. The output common mode voltage is stabilized to $V_{dd}/2$ by the simple loop based on amplifier A_{CMFB}.

3. Analysis of non-idealities

3.1. Finite frequency bandwidth

As far as bandwidth is concerned, we recall that it is necessary to maintain a flat frequency response over the required frequency range up to the demodulator input. The elements that dominate the frequency response are depicted in Fig. 4(a), showing the differential mode representation of the left half of the amplifier. The input signal, V_Y, is transferred to V_X by a low pass transfer function, with upper band limit equal to the 0-dB frequency (f_0) of the OTA-L/M_{1L} composite op-amp.

The M_{1L}-M_{11L} series supplies the whole ac current exiting V_X node. This current includes the correct contribution, which flows into resistor R_{1L}, and an error component, which flows into parasitic capacitances (represented by C_{pX}) and into the C_C, R_C series. Assuming that $i_{d2} = i_{d1}$:

$$i_{d2} = \frac{v_y}{R_{1L}} \frac{1 + j\frac{f}{f_Z}}{1 + j\frac{f}{f_0}} \tag{2}$$

By means of simple calculations and neglecting the zero nulling resistor R_C, we can find the following approximations for f_0 and f_Z:

$$f_0 \cong \frac{g_{m-in}}{2\pi\left(C_C, + , \frac{C_{pA}}{g_{m-2L}R_{1L}}\right)} \tag{3}$$