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Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS

Matteo Avoli, Francesco Centurelli, Pietro Monsurrò, Giuseppe Scotti*, Alessandro Trifiletti

DIET (Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni), University of Rome "La Sapienza", Italy

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ABSTRACT

The low power instrumentation amplifier (IA) presented in this paper has been designed to be the front-end of an integrated neural recording system, in which common-mode rejection ratio (CMRR), input referred noise and power consumption are critical requirements. The proposed IA topology exploits a differential-difference amplifier (DDA) whose differential output current drives a fully differential, high-resistance, transimpedance stage, with an embedded common-mode feedback loop to increase the CMRR. This stage is followed by a differential-to-single-ended output amplifier. Low-power operation has been achieved by exploiting sub-threshold operation of MOS transistors and adopting a supply voltage of 1 V. Simulation results in a commercial 65 nm CMOS technology show a 1 Hz to 5 kHz bandwidth, a CMRR higher than 120 dB, an input referred noise of 8.1 μVrms and a power consumption of 1.12 μW.

1. Introduction

The accelerating development of research in neuroscience generates an increasing interest in neural recording systems able to monitor the activity of large groups of neurons. Integrated circuits designed to interface microelectrode arrays implanted in the brain and to process neural signals are key components to treat neurological disorders, such as epilepsy and Parkinson's disease, and to speed up the research in the field of brain-machine interfaces (BMIs) [1–5]. The typical neural microsystem is composed of a microelectrode array [5], implanted in the brain tissue, connected to a front-end amplifier, which is the first stage of the data processing chain. It is followed by an additional amplifier/filtering stage driving an analog-to-digital converter (ADC), some digital signal processing functions and an RF transmitter to send data out of the body. This single processing chain is replicated many times to create an array of several neural microsystems to monitor several neurons simultaneously [2,6–9].

The main specifications to be considered in the design of IAs for neural recording applications are: high differential gain, high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), low input referred noise (IRN), high input impedance, low power consumption and small area footprint. The bandwidth needed to process neural signals is less than 10 kHz (5 kHz in most cases), and the need to reject large dc offset voltages caused by the electrode material and the shape of the recording site requires ac coupling of the input, with a cut-off frequency in the order of 1 Hz.

The neural signals to be measured are very weak (in the order of 10–100 μV), thus requiring high gains and very low sensitivity to noise and disturbances: hence the requirements on CMRR, PSRR and noise. Low IRN in particular is a key requirement, despite of the introduction of advanced neural electrodes that allow achieving larger input signals. The main noise contributions come typically from the noise sources in the input stage of the IA; to reduce their influence, the transconductance of the input MOS devices has to be large, which requires large aspect ratios and bias currents. The optimal trade-off between IRN and power (and area) consumption has to be found at design time.

The equivalent impedance of commercially available electrodes is in the order of 100 kΩ [5,10], and this requires a large input impedance for the front-end amplifier, to minimize input signal partition. Low power consumption is a key requirement, since the temperature of the integrated circuit implanted in the brain must be kept low, to avoid damaging the tissues, and small area footprint is required to ease the integration of multiple neural recording channels on the same chip.

There are several architectures of instrumentation amplifier suitable for neural recording applications. Among them we mention the 3-OPA IA, the current-balancing IA (CBIA) [11,12], the OTA-based IA [7,8,13–15] and the DDA-based IA [16,17]. The 3-OPA (operational amplifier) IA is the less suitable architecture for neural recording applications, since good CMRR performance requires a very good matching between several feedback resistors, which is difficult to achieve in nowadays nanometer CMOS processes. The CBIA exhibits good CMRR performance without requiring matched resistors, but its

* Corresponding author.
E-mail addresses: centurelli@diet.uniroma1.it (F. Centurelli), monsurro@diet.uniroma1.it (P. Monsurrò), scotti@diet.uniroma1.it (G. Scotti), trifiletti@diet.uniroma1.it (A. Trifiletti).

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PSRR performance is poor and the architecture is not suitable for ac coupling. OTA-based IAs are the most used for neural recording applications; since their topology is very simple; they require, in principle, the lowest area and power consumption, but their performance in terms of CMRR, PSRR and input impedance is worse than for the other architectures. The OTA (operational transconductance amplifier) topology proposed in [13] is very simple, based on a conventional symmetrical OTA with the addition of cascode transistors in the output branch to enhance the open-loop gain. This design achieves good performance in IRN and area footprint, but power consumption is much higher than in similar designs. The front-end architecture proposed in [15] is based on a very simple OTA topology, but the conventional single feedback capacitor is replaced with a clamped T-capacitor network, thus improving the trade-off between input impedance and chip area. The IA architecture proposed in [7] is composed of a preamplifier connected to a band-pass filter. The current splitting technique is combined with an output branch current scaling strategy to improve the noise and power consumption trade-off. The DDA-based (differential-difference amplifier) IA has been sometimes used since it requires just two passive components, whose matching affects gain and not the CMRR, and CMRR performance is related only to the mismatch of the input ports [16].

The IA architecture proposed in this work is based on a DDA configuration similar to [17]; a different solution is proposed to achieve ac coupling without degrading noise performance, and the internal topology of the amplifier is modified by using a fully differential folded cascode input stage with an additional CMFB to enhance open-loop gain and strongly improve CMRR performance with respect to conventional IAs for neural recording applications. The amplifier has been designed in a commercial 65 nm CMOS process with a supply voltage of 1 V. The paper is structured as follows: Section 2 presents the adopted closed-loop configuration showing how to achieve a good trade-off between ac coupling and IRN requirements. In Section 3 we present the detail of the proposed IA topology and include simple design equations for differential-mode and common-mode frequency response as well as for input referred noise. The presented equations are suitable for pencil-and-paper calculations and provide insights into the main design choices to optimize IRN. In Section 4 we present the detailed design of the IA and simulation results, as well as comparison with the state of the art. Finally, some conclusions are presented in Section 5.

2. Closed-loop instrumentation amplifier configuration

The closed-loop configuration for a DDA-based IA proposed in [17] is shown in Fig. 1, where ac coupling is implemented through the capacitor C_1. In order to obtain a cut-off frequency f_L of about 1 Hz by using reasonable values of C_1 (e.g., lower than 10 pF), very large values

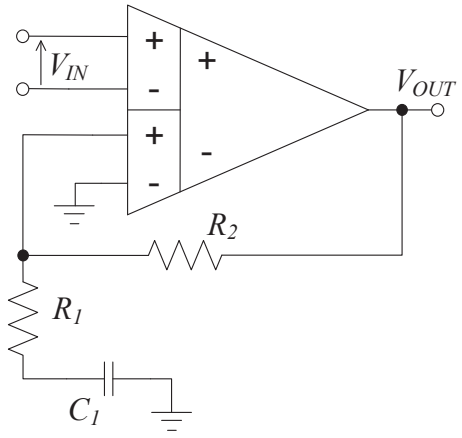

Fig. 1. DDA-based IA closed-loop architecture in [17].

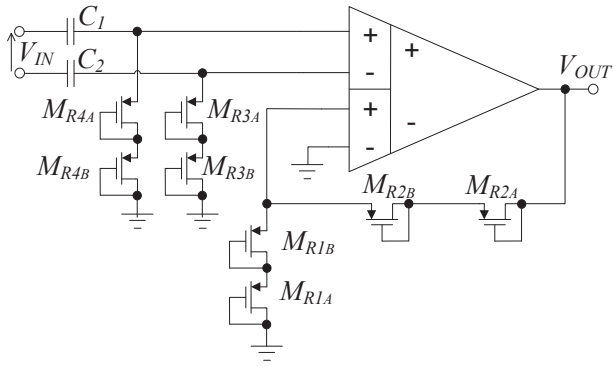

Fig. 2. IA configuration proposed in this work.

of R_1 and R_2 are required, in the order of GΩ However, such large resistors are not the ideal choice from a noise point of view, as will be demonstrated in the next Section.

The closed-loop instrumentation amplifier configuration proposed in this work, shown in Fig. 2, decouples ac coupling and feedback, solving this trade-off. We use MOS pseudo-resistors to close the external loop, since they provide better matching and lower area consumption than poly-Si resistors. Since noise is a critical specification for the instrumentation amplifier in general and in particular for neural recording applications, we have to keep R_1 and R_2 small enough that their noise contribution is negligible with respect to the noise sources within the DDA. AC coupling is implemented through capacitors C_1 and C_2 and resistors R_3 and R_4 (implemented through M_{R3A}, M_{R3B}, M_{R4A}, M_{R4B}), needed to set the input dc voltage; setting C_1 and C_2 at 3.5 pF, a cut-off frequency f_L below 1 Hz is obtained by sizing R_3 and R_4 at about 100 GΩ. It has to be noted that such a large value for resistors R_3 and R_4 results in a negligible noise contribution.

3. The proposed instrumentation amplifier topology

The internal block scheme of the proposed instrumentation amplifier is shown in Fig. 3. Two fully differential transconductors G_M are used to read the input and the feedback signals; their output currents are summed and drive a fully differential high-resistance transimpedance stage T_Z, with an embedded common-mode feedback (CMFB) loop to set the dc output voltage at nodes A and B and improve CMRR. This is followed by a differential-to-single-ended converter output stage A_V, providing further gain.

The input transconductors and the transimpedance stage are implemented as a folded cascode differential-difference amplifier (DDA), as shown in Fig. 4, where the detailed schematic of the proposed IA is presented. PMOS devices M_1-M_4 are used for the transconductors G_M for their better noise behavior. A DDA-based CMFB [18], shown in Fig. 5, controls the current sources M_{11} and M_{12} to keep the output common-mode voltage equal to the reference voltage V_{REF}. The current mirror load of the CMFB auxiliary amplifier allows achieving a gain of $g_m r_o$, thus improving the CMRR of the overall IA; higher gain, for instance by cascoding the DDA and the current mirror, would create stability issues and has been avoided.

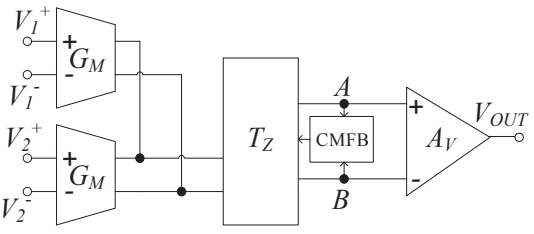

Fig. 3. Topology of the proposed DDA-based Instrumentation Amplifier.