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A Ka-band low power consumption MMIC core chip for T/R modules

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ABSTRACT

This paper presents a Ka-band low power consumption MMIC core chip using commercial 0.15 μm D-mode GaAs pHEMT technology for T/R modules. The core chip consists of two linear gain amplifiers, a SPDT switch, a 5-bit attenuator and a 5-bit phase shifter with a size of 4.8 mm × 2.5 mm. In the receiving mode, the 32–38 GHz core chip results in a gain of 9.0 dB and an output P_{1dB} of –3 dBm. In the transmitting mode, the gain and output P_{1dB} are 11.5 dB and +0 dBm, respectively. The measured rms attenuation error and phase error are 0.7 dB and 3.8°. The power consumption is 150 mW in both work modes. The measured results show that the operating bandwidth, power consumption, gain, rms attenuation error and phase error have been significantly improved compared with the previous reports.

1. Introduction

Compared with the traditional mechanically steerable antenna, active phased array antenna has a series of advantages such as fast scanning speed, various scanning modes, high reliability and easy maintenance. Recent years, the Ka-band active phased array antenna shows strong demand in the areas of satellite communications, data links and military radars [1]. T/R modules are the core components of the phased array antenna, they are usually composed of a number of MMICs into a microwave circuit to achieve signal amplification, transmitting and receiving mode conversion, amplitude and phase control functions. In order to complete the above functions, a chipset including the transmit and receive amplifiers, T/R switch, digital attenuator, digital phase shifter is often required [2–4].

However, this integration method leads to several issues, such as cost, size, reliability and consistency. As the size of the antenna array continues to grow, the number of T/R modules installed is also greatly increased. Therefore, core chip is emerging as a way to increase the integration, improve reliability and consistency, reduce cost and size. To date, core-chips below Ku-band have shown good performance. Some of them have completed reliability tests [5–7]. But when applied to Ka-band (above 26 GHz), the electromagnetic interference between circuits becomes more serious, and the performance such as operating bandwidth, phase shift and attenuation accuracy deteriorates significantly [11–13]. The compact Ka-band core-chip presented in this paper aims to solve the above problems and reduce power consumption through circuit topology design and layout optimization. The larger operating bandwidth and lower power consumption can well meet the application requirements of satellite communications, data links, etc.

In the following, the circuit topology design, EM simulation results of the Ka-band core-chip will be presented, together with the measurement results and comparison to the previous reports.

2. Design and fabrication

The functional circuit of the core chip consists of five parts: transmitting amplifier, receiving amplifier, 5-bit digital attenuator, 5-bit phase shifter and SPDT switch. For most phased array antennas, the transmitting channel does not need to adjust the power level through the attenuator. Therefore, we place the attenuator before the SPDT switch and after the receiving amplifier in order to increase the gain of the transmitting channel. As a result, the noise figure of the receiving channel will be improved. Amplifier and SPDT switch share +5 V power supply. Attenuator and phase shifter are both controlled by 5 bit parallel digital signal (0/−5 V). The functional block diagram of the core chip is shown in Fig. 1.

2.1. Amplifier

The transmitting/receiving amplifier has three cascaded transistors, ensuring that the amplifier provides at least a small signal gain of 21 dB and output P_{1dB} of 12 dBm (see Figs. 2 and 3). For the circuit design, a self-bias structure is adopted at the source to cancel the negative power supply requirement. While providing the easy power control, it also can better improve the stability of the amplifier, and minimize the loss of gain. The input, output and intermediate impedances matching are all

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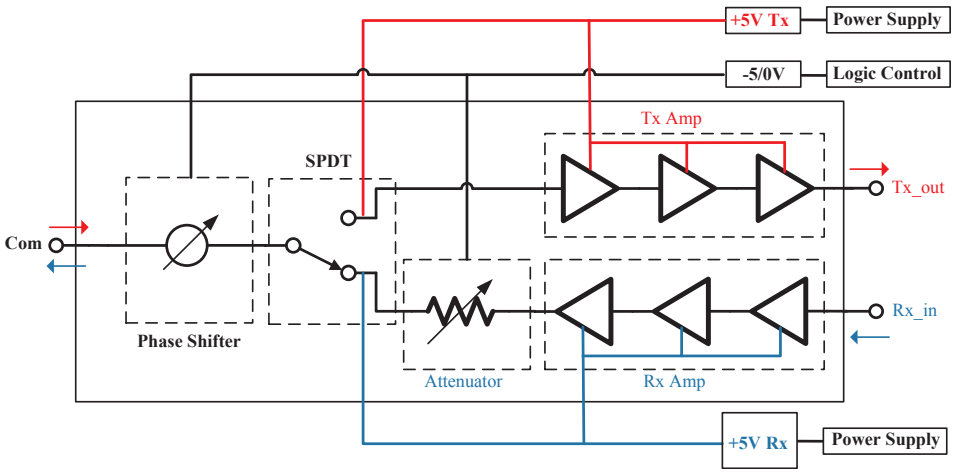

Fig. 1. Functional block diagram of core chip.

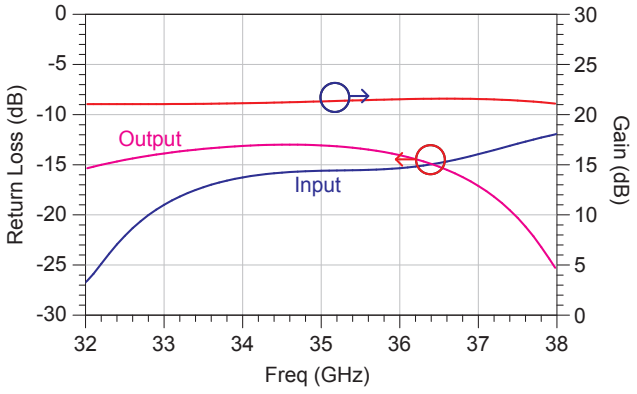

Fig. 2. EM simulated gain & return loss of amplifier.

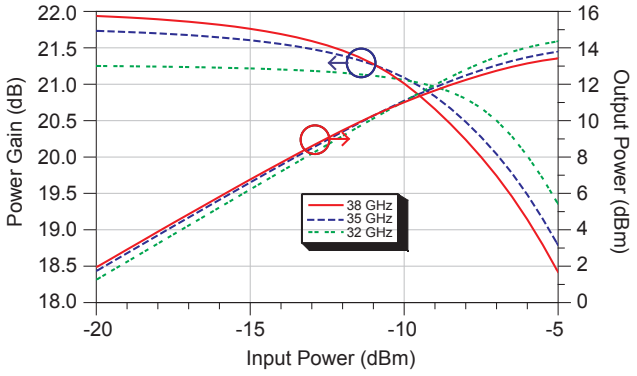

Fig. 3. EM simulated power characteristic of amplifier.

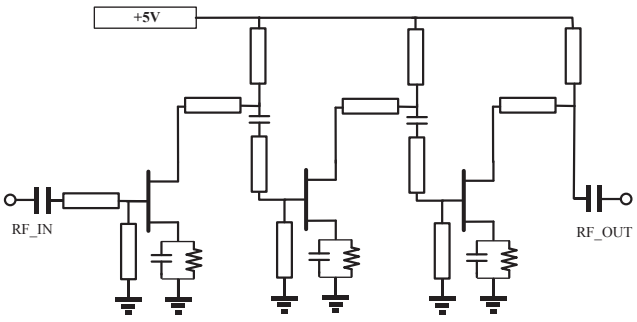

Fig. 4. Schematic of 3 stage self-bias amplifier.

finished by distributed components. The MIM capacitor is only used for DC block. For Ka-band chip, the EM simulation accuracy of distributed components is obviously higher than that of lumped components, and the insertion loss is also smaller. Therefore, other microwave circuits in this paper will refer to similar guidelines for design. The circuit topology of the amplifier is shown in Fig. 4.

2.2. SPDT switch

Commonly, we need at least a pair of control pad for channel switching [8]. For the normal operation mode of the T/R module, the SPDT control signal must be switched when the power signal of working status channel is turned on. Therefore, it is possible to replace the switch control signal with the power signal. Fig. 5 is the SPDT circuit topology. It adopts the structure of three parallel switch transistors. The gate is connected to the ground through a 20 kΩ resistor. Large resistance can guarantee the isolation of gate and source. We put a DC block capacitor on both end of the path to ensure the stability of the drain voltage. For instance, when the power signal is switched to the transmitting path, the gate to drain voltage $V_{GD} = -5V$. Then the switch transistor is off and the path turns on. When the power signal is switched to the receiving path, $V_{GD} = 0V$ means the parallel transistor is on and the path turns off Figs. 6 and 7 show the EM simulated results.

2.3. Attenuator

The 5-bit attenuator is composed of 0.5 dB, 1 dB, 2 dB, 4 dB, and 8 dB attenuation cells. LSB is designed as simple switched-T configuration. Other cells are designed as Lange coupler structures. The switched-T and bridge-T configurations are common used for attenuator [9], significant phase modulation effect due to asymmetry will seriously affect the performance of the attenuator in Ka-band. If matched components are used for phase compensation, the band width of the circuit will be significantly affected. Fig. 8 structure can be a good method to avoid this problem. The area of Lange coupler will be greatly reduced due to the frequency increase, which can be easily integrated. When the two symmetrical transistors connected to the transmit and coupled ports are turned off, the RF signal is completely reflected and synthesized at the isolated port, only a small part of the energy is lost through the transmission line. When the transistors are turned on, part of the RF signal leaks to the ground, part of the signal is reflected to the isolated port. This is how we control the signal to a specific amount of attenuation. Adjusting the gate width of the transistor will precisely