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−31 dBm sensitivity high efficiency rectifier for energy scavenging

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ABSTRACT

RF energy scavenging is capable in converting RF signals into electricity and has become a promising solution to power energy-constrained wireless networks. However, it has low power conversion efficiency especially when the harvested RF power is small. For this reason, we propose an enhanced differential-drive rectifier to improve the efficiency and the sensitivity of rectifier for energy scavenging applications. The proposed rectifier achieves dynamically controlled threshold voltage and reduces leakage current in the transistors through DTMOS transistor in differential-drive topology. The voltage boosting circuit further increases the sensitivity through step up the input signal before the signal enters the rectifier. The decoupling capacitor shunts the noise of the input signal before the signal is injected into the cross-connected gate reducing the voltage drop and maintaining the PCE of the rectifier. The rectifier is designed based on the 0.18 μm Silterra CMOS process technology. Effects of decoupling capacitors, voltage boosting circuit and output load on PCE of the rectifier have been evaluated. Technology scaling and parasitic effects to the rectifier have also been presented. Performance of N-stages proposed rectifier has been compared with the conventional BTMOS rectifier. The proposed method achieves the highest sensitivity of −31 dBm for 1, 3 and 5 stages rectifiers without the need of off-chip load capacitor.

1. Introduction

The growing use of portable electronic devices has increased the importance of recharging or replacement of batteries. As the technology advances, the use of battery to power the devices becomes inappropriate and is impossible for some cases due to their applications such as implantable medical devices. Thus, energy harvesting application is introduced and has become topic of interest in the development of microelectronics technology. Energy harvesting or energy scavenging operates by capturing the energy from surrounding (such as solar power, and thermal energy) and convert the received energy into electrical to power the electrical or electronic devices. RF energy harvesting is one of the most practical ways in low power applications. Since the source of energy is an AC sinusoidal signal, a rectifier is required to convert the AC source into direct current type. Rectifier usually produces low output voltage due to the nature of antenna to capture small energy. Thus, a high efficiency rectifier plays an important role to design an efficient energy harvesting system.

In previous research work, most of the rectifier design focuses on the optimization of power conversion efficiency (PCE) and the output voltage only [1]. While it is important to maximize the PCE, the sensitivity of the rectifier should also be put into consideration to provide broad range of very low RF input power so that the system can still operate when very little voltage or energy is present in the ambient environment [2].

Differential-drive rectifier (DDR) is known for its ability to provide small turn-on voltage and leakage current simultaneously which is beneficial in designing high efficiency rectifier. Dynamic threshold voltage MOSFET (DTMOS) diode-connected transistor is used to further decrease the threshold voltage (V_{th}) which helps in increasing the sensitivity. A grounded capacitor at each of the cross-connected gate-to-drain terminal and an off-chip inductor-capacitor (LC) voltage boosting circuit at each of the rectifier input are applied to further increase the sensitivity of the rectifier. A 50 Ω impedance matching network is used to ensure maximum energy captured by the antenna is transmitted to the main circuit.

The paper is organized as follows: Section 2 introduces the architectures and the characteristics of both conventional body-tied-to-source MOSFET (BTMOS) and DTMOS rectifier designs. Section 3 discusses the design and characteristics of the proposed rectifier. Section 4 presents the simulation results and discussions of the simulated rectifier followed by the conclusion in Section 5.

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2. Rectifier topologies and its characteristic

2.1. BTMOS and DTMOS transistor

Half-wave, full-wave and bridge rectifiers are the basic designs of rectifier to convert AC source into DC. It comprises of PN junction diodes which have relatively high turn-on voltage, usually 0.7 V to 1 V, making it not suitable for low power application. The alternative way to design this rectifier is by using Schottky diode due to its characteristics that has low V_{th}, low conduction resistance and very fast switching speed [3]. However, it suffers from reverse leakage current and is not compatible with the standard CMOS process. The implementation of it will lead to extra cost of fabrication which is undesirable [4].

In CMOS technology, the diode can be replaced by connecting the gate terminal to the drain terminal to form a diode-connected MOSFET. This type of transistor is known as BTMOS diode. In BTMOS, the substrate is usually connected to the source terminal as shown in Fig. 1(a). As diode D1 is shorted, the total current flow through the transistor is the total of channel current plus the current flow through parasitic diode D2. During reverse bias operation, high reverse current flows through the transistor due to the direct current flow in the parasitic diode [5]. As the reverse bias voltage increases, the reverse current also increases exponentially. This leads to degradation in the rectifier efficiency. Authors in [5] proposed a technique where the V_{th} of MOSFET can be controlled dynamically by connecting the substrate to the gate instead to the source.

Since the substrate and the gate are tied together, the body-to-source voltage (V_{bs}) is driven by the gate-to-source voltage (V_{gs}). Thus, V_{gs} is equal to V_{bs}. When $V_{gs} = V_{bs} = V_{max}$ (amplitude of input signal), the source and the substrate is in forward bias forcing the V_{th} to drop. When $V_{gs} = V_{bs} = 0$, the V_{th} is high, causing the leakage current to reduce and turn-off the transistor completely. The relation between input signal and V_{th} is described in Eq. (1), where $2\phi_B$ is the inversion layer potential, V_{FB} is the flat band voltage, and γ is the body effect factor [6]. From (1), as the V_{bs} increases, the V_{th} would decreases. V_{th} will decrease until $V_{gs} = V_{bs}$ reaches $2\phi_B$. The current drive of DTMOS is also higher than the conventional BTMOS. Fig. 1(c) and (d) explains the characteristics of the BTMOS and DTMOS configurations.

$$V_{th} = 2\phi_B + V_{FB} + \gamma(\sqrt{2\phi_B - V_{bs}}) \quad (1)$$

The efficiency of the rectifier is determined by few factors including V_{th}, leakage current, on-resistance (r_{-on}), input amplitude, etc. At very low input power, the turn-on voltage of transistor will be higher than the V_{gs}. In this state, the transistors will work in subthreshold or in cut-off region. Thus, the efficiency is very poor at very low input power [7]. To obtain high efficiency rectifier, the V_{th} and leakage current of the transistor should be small [8]. Rectifier efficiency can be defined by the PCE factor as in Eq. (2) where P_{loss} is the conduction power losses in the rectifier.

$$PCE, \eta\ \% = \frac{Pout}{Pin} = \frac{Pout}{Pout + Ploss} \times 100 \quad (2)$$

Differential-drive based rectifier proposed by authors in [9] consists of 4 transistors with cross-connected gate structure to form a complimentary bridge rectifier as shown in Fig. 2(a). Differential input signal is increased by pump capacitor (C_P) and is applied across the two nodes, V_x and V_y. This signal is then transferred to the cross-connected gate of the rectifier. The V_{gs} of the transistors is driven by the voltage applied at node V_x and V_y. When positive voltage is applied to the node V_x, M_{n2} and M_{p1} are in forward bias. In this situation, these devices will act as small r_{-on}. The transistors will turn-on when V_x reaches the V_{th}. The positive voltage applied at the gate of M_{n2} causing the V_{th} of these devices reduces effectively. During this cycle, M_{n1} and M_{p2} operate in subthreshold region [10]. On the other hand, when negative voltage is applied at node V_x, M_{n2} and M_{p1} will operate in reverse bias. Since the gate voltage of M_{n2} is negative, the V_{th} will increase, reducing the reverse leakage current. By using this rectifier topology, both the low V_{th} and leakage current can be achieved simultaneously [3,9]. DTMOS DDR operates in the same way as the BTMOS DDR excepts the bulks in DTMOS is connected to the gate instead to the source terminal as explain in Section 2.1. Low V_{th} in DTMOS DDR increases the sensitivity and the PCE of the rectifier.

In low power applications, the transistors should operate in subthreshold region [1]. Therefore, the output voltage will be different

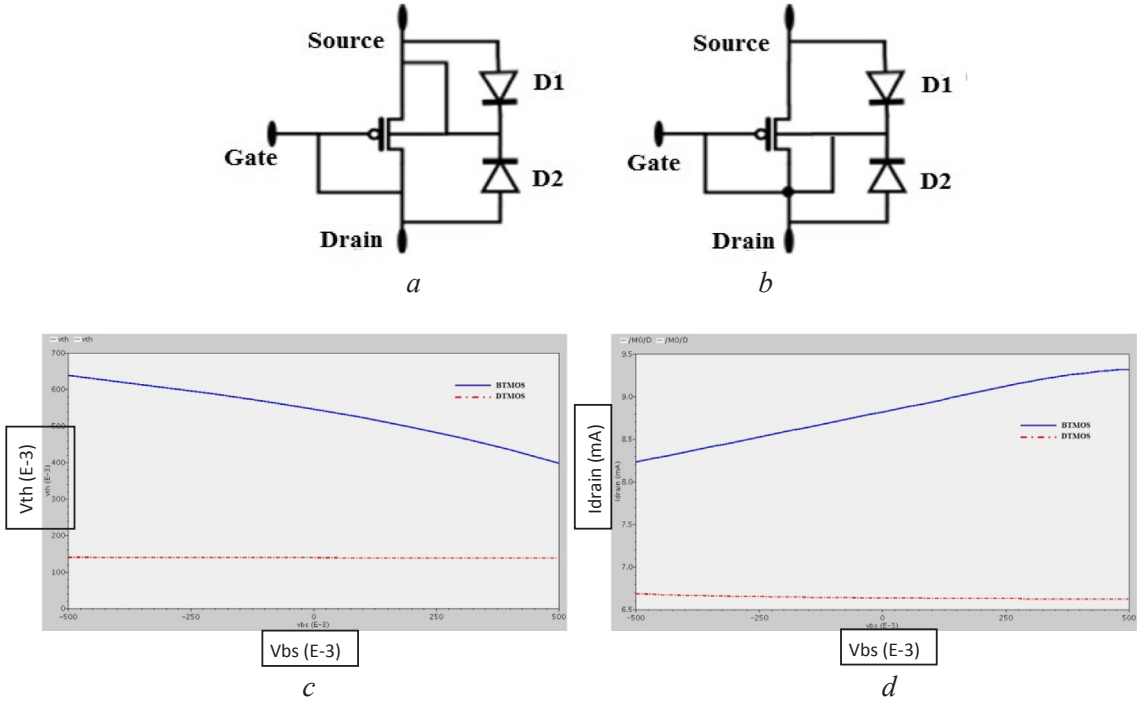

Fig. 1. BTMOS and DTMOS diode MOSFET architecture and characteristics against V_{bs} at NMOS w/l = 14 µm/180 nm and V_{dd} = 1.8 V. (a) BTMOS diode, (b) DTMOS diode, (c) V_{th} vs. V_{bs}, (d) I_d vs. V_{bs}.