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Low-voltage PVT-insensitive bulk-driven OTA with enhanced DC gain in 65-nm CMOS process

Harikrishna Veldandi*, Rafi Ahamed Shaik

Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, Guwahati 781 039, India

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ABSTRACT

This paper presents a high DC gain bulk-driven operational transconductance amplifier (OTA) for low voltage applications. A cross-coupled active load is employed at the bulk-driven input stage to enhance the gain of OTA. A cross-forward (CF) gain stage was placed between the input and output stages of the OTA to enhance the output stage transconductance. The CF stage improves the phase margin of OTA and keeps the amplifier stable even for large capacitive loads (up to 50 pF) and also improves overall DC gain. The proposed OTA simulated using UMC 65-nm standard CMOS process, operates at a supply voltage of 0.5 V. Simulation results show that the OTA provides a gain of 72 dB at very low-frequencies. It has a phase margin of 74° and a unity gain frequency of 680 kHz for a load capacitance of 20 pF. Because of the bulk-driven input stage, the OTA achieved rail-to-rail input common-mode range. When the OTA simulated with a supply voltage of 0.35 V and load capacitance of 20 pF, the OTA provides a DC gain of 55 dB and a phase margin of 68° at a unity gain frequency of 617 kHz. The power dissipations were 3.03 μW and 1.56 μW for supply voltages of 0.5 V and 0.35 V, respectively. In comparison to previous works, the figure of merit of the proposed OTA has more than doubled in all respects.

1. Introduction

In the recent years, the demand for emerging battery-operated portable and wearable electronics devices such as mobile phones, music players, and biomedical instruments (hearing aids, implantable cardiac pacemakers and heart-rate detectors) has been increasing. Most of these applications use system-on-chip (SoC) that consists of analog, digital, and intrinsic mixed-signal circuits. In order to extend the battery life in these systems, their design should be more power efficient. Also, the system should be able to operate with a low voltage (LV) supply. Moving towards thin-oxide sub-nanometer CMOS technology entails the use of low supply voltages to ensure device reliability. However, the threshold voltage (V_{th}) of MOS devices is not scaled down at the same rate as that of the power supply, in order to limit their leakage currents. Low-V_{th} device and low-supply voltage benefit digital circuits in terms of higher speed, better integration and power efficiency. On the other hand, short channel effects and other higher-order effects degrade the analog circuits performance. Because of these effects, it becomes difficult to achieve the design specification targets such as linearity, gain, and speed with low power consumption [1]. Also, due to the reduced voltage headroom, the design of analog and mixed-signal circuits becomes highly challenging. To overcome the above problems, a number of innovative LV design techniques have been developed in recent years, such as those based on level shifter, bulk-driven (BD), floating gate (FG), self-cascode, and design in sub-threshold region [1,2].

Most of the analog and mixed signal integrated circuits include operational transconductance amplifiers (OTA). Often, these OTAs are the most power hungry blocks applications such as pre-amplifiers, integrators, switched capacitor circuits, analog filters, and data converters. For these applications, the OTA is required to have high DC gain, high speed, high slew rate, linearity, and process, voltage and temperature (PVT) insensitive.

However, the conventional gate-driven techniques are suitable for the design of high gain and low noise amplifiers. But, these circuits offer limited common-mode input range under low-voltage condition, due to threshold voltage limitation in signal path. There are many traditional design approaches for implementing a low-voltage transconductance amplifier to increase the input common-mode range. By using a complementary input stage [3–5], or by using dynamic level shifters [6], the input range can be extended. But complex bias circuits are required to minimize the dead zone in the input range. By employing floating-gate MOS devices [1], the input common-mode range can be improved, but the noise performance degrades. Also, the residual charge on the floating gate has a widely varying effect on the circuit performance [7–9].

In such LV applications, the BD-MOSFETs are preferred over their

* Corresponding author.
E-mail address: h.veldandi@iitg.ernet.in (H. Veldandi).

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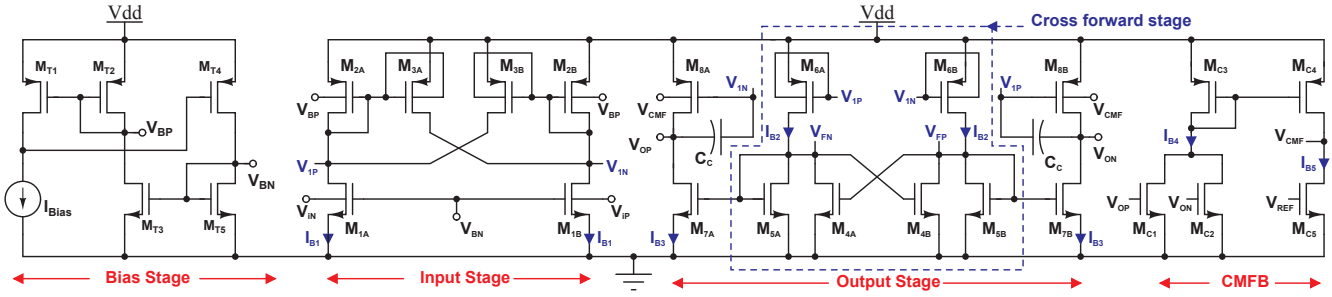

Fig. 1. Schematic of the proposed pseudo-differential OTA.

gate-driven counterparts. The former help to achieve rail-to-rail input operation since these MOSFETs allow a large input signal range without shifting into the cut-off region [10]. However, the bulk-source transconductance (g_{mb}) is smaller than the gate-source transconductance (g_m) and it is not sufficient to achieve a large DC gain and a gain-bandwidth product.

Hence, novel techniques are required to overcome the demerits of BD-MOSFET. In recent years, many LV circuits utilising BD-MOSFETs such as differential amplifiers [10–30], current mirrors [31], voltage references [32] and buffers [33–36] have been presented, showing improved performance under low-voltage operation.

Various solutions have been proposed in the literature to improve the performance of BD-OTAs for sub-1 V supply, mostly targeting an improvement in the DC gain. These solutions do have their merits and demerits. BD folded-cascoded architecture employs an array of self-cascode transistors to improve the gain [11]. Current recycling has been used to improve transconductance of BD input stage [12–15]. However, these approaches are not suitable for sub-1 V design because the cascode structure limits the signal swing. The BD flipped voltage follower has been employed at the input stage to improve the linearity and dynamic performance of OTA [16]. In [17], a multi-signal path input stage is employed to enhance the transconductance of folded-cascode topology.

Some sub-1 V BD architectures based on two-stage topology were proposed in order to save power and minimize the compensation task [18–20]. But these circuits provide limited gain and require more power to achieve higher unity gain bandwidth (UGB). To overcome this, some researchers proposed the concept of partial positive feedback to enhance transconductance with a small amount of current [10,21–24]. In addition, auxiliary blocks such as differential amplifier [22,25], current-shunt amplifier [26] were also employed to improve the transconductance. Other reported designs use a three-stage topology to further enhance the gain and bandwidth of OTA [27–29]. These circuits need a complex compensation network such as nested miller compensation network or damping factor controlling network to improve the load driving capability. The design in [28], employed local common mode feedback (LCMFB) with the help of a resistor to improve the dynamic performance i.e., slew rate. The design in [29] is based on a self-biased circuit to improve the common-mode and power-supply rejection of the OTA.

Some of the designs proposed in literature do not meet the low-voltage condition [12–15]. In a few other cases, the circuit performance does not remain constant with PVT variations [10,16,21–24]. Some of the existing topologies, though suitable for low-supply voltage, come at the cost of additional power and area [28,29]. Hence, there is a need for new topologies which work with sub-1 V supplies and meet all the specifications of OTA with a smaller quiescent current and PVT insensitivity. This article presents a solution to a BD-OTA for low supply voltage, to obtain adequate DC gain without giving up on other performance parameters of the OTA such as UGB, slew rate, and output swing.

The proposed high gain OTA design is based on a pseudo-differential topology is able to work with sub-0.5 V supplies. The circuit is designed in a 65 nm CMOS technology. All the MOSFETs in the proposed design operate in weak inversion. The gain of the BD input stage is improved with the help of partial positive feedback technique. An additional cross-forward (CF) stage assists in increasing the gain of second stage. It also improves the driving capability of OTA without any stability issue. The proposed design can drive capacitive loads of up to 50 pF, with only a minor reduction in phase margin.

This paper is arranged as follows: Section 2 describes the architecture and operation of the proposed OTA. The analysis of various performance parameters and frequency compensation is discussed in Section 3. Simulation results of the proposed OTA are presented in Section 4 and the performance of proposed work in comparison to the state-of-the-art is discussed in Section 5. Section 6 gives the important conclusions drawn from this work.

2. Pseudo-differential bulk-driven OTA

Schematic of the proposed bulk-driven OTA is shown in Fig. 1. All the transistor pairs are symmetrical, with each transistor having its counterpart in the opposite branch. They all operate in the weak inversion region and are biased at mid-of-supply voltage (i.e., $V_{DD}/2$) for desired bias current. In order to achieve maximum voltage swing, the input and output common-mode node voltages are set to $V_{DD}/2$. The input stage is designed using a Triple-well CMOS process with access to the bulk-terminal of nMOS transistor. The bulk terminals of some of the MOSFETs are biased at common-mode voltage in order to reduce the threshold voltage (V_{th}) of device which makes it easy to operate at low-voltages. The proposed OTA architecture constitutes input, output, and cross-forward stages. In addition, a common-mode feedback (CMFB) circuit is employed for the output stage. It will help in keeping the output common-mode node voltage to a known reference value (V_{REF}).

2.1. Input stage

A bulk-driven pseudo-differential pair is employed as the input stage of OTA and it consists of transistors $M_{1A,B}$–$M_{3A,B}$. Differential inputs V_{iN} and V_{iP} are applied across the bulk terminal of M_{1A} and M_{1B}. The input stage loaded with diode connected pMOS transistors M_{2A}–M_{2B}. Another pair of pMOS transistors, M_{3A}–M_{3B}, is configured in a cross-coupled mode to cancel gate transconductance and it enhances the gain of input stage. The bulk terminals of M_{3A}–M_{3B} are also connected in a cross-coupled manner, which helps in further improvement of gain. Under differential input signal, the cross-coupled pair acts in partial positive feedback mode and gives a negative transconductance and the overall load conductance will be reduced. This results the differential-mode gain of the first stage to be set at a high value. With a common-mode input signal, the operation will be vice versa.

The sub-threshold current-voltage (I-V) relations of MOS transistor operating in the weak inversion region is given by [37]