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A 5-bit 1.8 GS/s ADC-Based Receiver with Two-Tap Low-Overhead Embedded DFE in 130-nm CMOS

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***Abstract*—Along with CMOS technology scaling, ADC-based serial link receivers have drawn growing interest in backplane communications but power dissipation of the ADC and complex digital equalizer in such digital receivers can be a limiting factor in high-speed applications. Implementing analog embedded equalization within the front-end ADC structure can potentially relax the ADC resolution requirement and reduces the complexity of the DSP which results in a more energy-efficient receiver. In this paper, the equivalence between the speculative comparisons of a loop-unrolling DFE and an ADC with non-uniform quantization levels is utilized to propose a novel ADC-based DFE receiver structure. The equivalency partially compensates for the power overhead imposed by loop-unrolling DFE. The 5-bit prototype receiver with two-tap embedded DFE is designed, laid out and simulated in a 130-nm CMOS process with 1.8 Gbps data rate. With embedded DFE disabled, the receiver achieves 4.57-bits ENOB and 1.77 pJ/conv.-step FOM. With 1.8-Gbps signaling across a 48-in FR4 channel, the two-tap DFE enabled receiver opens the completely closed eye and allows for a 0.26 UI timing margin at a BER of 10^{-9}. The total active area is 0.21 mm^2 and the ADC consumes 76 mW from a 1.2-V supply.**

Keywords: **Analog-to-digital converter; Serial link receiver; Decision feedback equalization (DFE); Analog DFE; Flash ADC.**

1. INTRODUCTION

The aggressive scaling of CMOS technologies over the past few decades has made it possible to realize complicated signal equalization algorithms in the digital domain that enables serial I/O links to operate reliably at 10 Gbits per second (Gb/s) and beyond over high-loss channels [1-5]. The use of an analog-to-digital converter (ADC) as the front-end stage of a link receiver to digitize the received signal, allows for the efficient implementation of the complex equalization algorithms, adopting advanced coding and modulation schemes, and better programmability and adaptability to different channel profiles. These features have generated an increasing trend towards the use of high-speed ADCs in the wireline communication over high-loss channels [6-10].

One of the main challenges for such ADC-based receivers is maintaining a reasonable power budget for the ADC and digital signal processor (DSP), especially with multi-giga samples per second (GS/s) sampling rates [11-13]. While the most state-of-the-art multi-GS/s ADCs suffer from high power dissipation even at moderate resolution of 6 bits, the post-ADC digital equalization circuitry can also have comparable power to the ADC [14]. These result in a higher overall power consumption for the ADC-based receivers that may be a prohibitive factor for their adoption in backplane receivers, compared with the binary approaches. However, recent developments in the implementation of power-efficient multi-GS/s ADCs, as well as low-power mixed-signal equalization approaches have led to realization of the receivers that fulfill the stringent power requirement of the serial links [7], [10], [15].

For a given target bit-error rate (BER), embedding analog decision feedback equalization (DFE) as one of the most powerful equalization technique can relax the ADC resolution requirement and allows for utilizing the digital equalization with lower complexity and power consumption [16,17]. But to implement an embedded analog DFE, the subtraction of post-cursor inter-symbol interferences (ISIs) from the current input should be completed before the arrival of the next sample, hence imposes a challenging feedback delay requirement. Loop-unrolling DFE improves the feedback delay by simultaneously comparing the input with all possible ISI values, while exponentially increasing the power consumption and area [18]. This paper describes a way of improving the performance of the incorporated ADC in an analog DFE receiver. It particularly suggests a receiver topology that relaxes the ADC requirements by directly using the decisions of the speculative comparisons of a loop-unrolled DFE and thus relatively compensates for its power and hardware overheads.

The rest of the paper is organized as follows. Section 2 briefly reviews the structures of the ADC-based DFE receivers. The equivalence between loop-unrolling DFEs, non-uniformly quantized ADCs, and the proposed ADC-based DFE receiver are presented in Section 3. In Section 4, the details of the circuit implementation of the proposed DFE receiver are provided. Simulation results are shown in Section 5 and conclusions are given in Section 6.

2. ADC-Based DFE Receivers

Fig. 1 shows the block diagram of an ADC-based receiver with two different DFE schemes: embedded analog DFE and post-ADC digital DFE. In analog approach, feedback equalizer subtracts the appropriate amount of offset from the un-quantized analog input for ISI cancellation. The ADC's decision-making and the DAC settling should be accomplished within one unit interval (UI), hence causing a stringent delay.

To mitigate this issue, the summation point can be moved into the digital domain (see Fig. 1). Therefore, the ADC is no longer in the DFE loop and the equalization process is performed completely in the digital domain. In the post-ADC DFE, a proper binary offset is subtracted from the ADC output based on the prior bit decisions. The resulting value is then compared with a threshold and a decision slicer retrieves the current bit. The moving of the DFE timing loop into the digital domain can be applied to the ADC-based receiver with embedded analog DFE.