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Ultra-high current efficiency single-stage class-AB OTA with completely symmetric slew rate

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ABSTRACT

An ultra-high current efficiency single-stage class-AB OTA with completely symmetric slew rate is presented. Based on adaptive biasing and nonlinear current mirror techniques employed in a proposed symmetric current recycling structure, the proposed OTA not only achieves the maximum output current proportional to Vin^8, but also has the symmetric positive and negative slew rates. Also, the proposed self-biasing output stage makes the slew rate unconstrained. Simulation results demonstrate that the slew rate of the proposed OTA is enhanced by 1500% over that of the conventional folded cascode counterpart with a little increased power, which is suitable for large capacitive load applications.

1. Introduction

In the low-voltage low-power switched-capacitor applications, especially for large capacitive load, operational transconductance amplifiers (OTA) with high slew rate and large gain-bandwidth product (GBW) are required [1]. Thus, enhancing the current efficiency (CE) of the OTAs has become prevalent in recent years. The conventional folded cascade(FC) OTA is the most commonly used amplifier structure, which is shown in Fig. 1. However, the CE is not large enough owing to its working at the class-A status. In order to enhance the CE of the FC, the current recycling technique is proposed [2–8]. However, the maximum output current of current recycling structure is limited by the tail current of input pairs. Thus, the slew rate is only linearly enhanced. To resolve this problem, some techniques have been presented, such as adaptive biasing [9,10], and nonlinear current mirror [11] and quasi-floating gate [12,13] techniques. These techniques significantly improve the maximum output current without the constraint of the tail current. Nonetheless, the maximum output current can only be achieved to be proportional to Vin^4 according to the published papers as of now. More importantly, because of the cascode transistors biased by constant voltage in the conventional output stage, the achievable maximum slew rate is limited, especially in the low-voltage applications.

To solve the above problems, an ultra-high current efficiency single-stage class-AB OTA with completely symmetric slew rate is presented in this paper. It employs adaptive biasing and nonlinear current mirror techniques in our proposed symmetric current recycling structure [14], achieving that not only the maximum output current is increased to be proportional to Vin^8, but also has the symmetric positive and negative slew rates. At the same time, our proposed self-biasing output stage dynamically bias the gate voltage of cascode transistors, making the slew rate unconstrained.

The following sections present the details of our proposed approach. In Section 2, the conventional FC OTA is summarized. In Section 3, we introduce each technique's details of our proposed OTA. In Section 4, the detailed circuit analysis is discussed. The performance comparisons of two OTAs, the conventional FC and our proposed OTA, are given in Section 5. And Section 6 gives the conclusions.

2. Conventional folded cascode OTA

The conventional folded cascode (FC) OTA is shown in Fig. 1. The equivalent transconductance (G_m) of the FC can be expressed as,

$$G_{m,FC} = g_{m,1} \tag{1}$$

where $g_{m,1}$ is the transconductance of the input transistor $M1$. Consequently, the GBW of the FC can be given as,

$$GBW_{FC} = \frac{G_{m,FC}}{C_L} \tag{2}$$

Meanwhile, the slew rate of the FC can be described as,

$$SR_{FC} = \frac{2I_B}{C_L} \tag{3}$$

Note that the slew rate of the FC can not achieve a larger value, which are limited by the tail current source ($M7$) and the folded current

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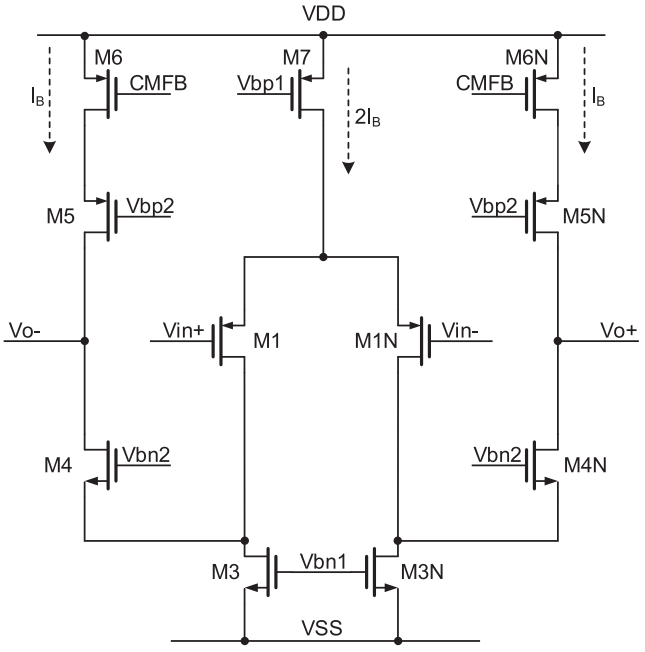

Fig. 1. The conventional folded cascode OTA.

sources (*M*3 and *M*3*N*), making the FC operate at class-A status.

3. Enhanced symmetric recycling OTA

The schematic of the proposed enhanced symmetric recycling OTA(ESRFC) is shown in Fig. 2. It consists of the adaptive biasing class-AB input stage, the symmetric current recycling structure composed of the nonlinear current mirror and the self-biasing output stage. The technique details are presented as follows.

3.1. Adaptive biasing class-AB input stage

The adaptive biasing class-AB input stage consists of the input differential pairs (*M*1*a*,*M*1*b*,*M*1*aN* and *M*1*bN*) and two cross-coupled Flipped Voltage Followers (FVFs) composed of the input transistors (*M*1*c* and *M*1*cN*), diode-connected transistors (*M*8 and *M*8*N*) and current sources (*M*9 and *M*9*N*). In dc conditions, the bias current for FVFs is set to $0.5I_B$. Owing to the matched input transistors of FVFs, the bias current of the input differential pairs is also $0.5I_B$. For small signal analysis, due to the effect of FVFs, the input signal is also applied to the source terminal of the input differential pairs, leading to a boost in the effective transconductance (G_m), which can be expressed as,

$$G_m = 2 \cdot g_{m,1a} \tag{4}$$

where $g_{m,1a}$ is the transconductance of the input transistor *M*1*a*. For the large signal response, when a large negative step signal happens at *Vin*+, due to the role of the FVFs, the voltage at node *Y* rapidly decreases, forcing the input transistors *M*1*aN* and *M*1*bN* to turn off. Instead, the voltage of node *X* does not change, making a large current I_{in} flowing through *M*1*a* and *M*1*b*, which can be expressed as,

$$I_{in} = \frac{\beta_{1a,b}}{2}\left(\sqrt{\frac{I_B}{\beta_{1a,b}}} + V_{id}\right)^2 \tag{5}$$

where $\beta_{1a,b} = \mu_n C_{ox}(W/L)_{1a,b}$ is the transconductance factor of transistors *M*1*a* and *M*1*b*, and V_{id} is the input differential signal. Therefore, the proposed input stage is operating at class-AB status.

3.2. Nonlinear current mirror

Transistors *M*3*a*−*M*3*b*−*M*3*c* form the nonlinear current mirror, so as the *M*3*aN*−*M*3*bN*−*M*3*cN*,*M*4*a*−*M*4*b*−*M*4*c* and *M*4*aN*−*M*4*bN*−*M*4*cN*. The bias voltage for *M*3*c* and *M*3*cN* are provided by *Vntri*, making *M*3*a* and *M*3*aN* at the margin of saturation region. So as the bias voltage *Vptri*. Take *M*3*a*−*M*3*b*−*M*3*c* as an example. When a large current I_{in} enters into *M*3*c*, the source voltage of it significantly decreases, forcing the *M*3*a* to work at the triode region. Thus,the current I_{3b} flowing through *M*3*b* can be expressed as,

$$I_{3b} = \frac{\beta_{3b}}{2}\left(\frac{I_{in} + 0.5I_B}{\beta_{3a} V_{ds,3a}}\right)^2 \tag{6}$$

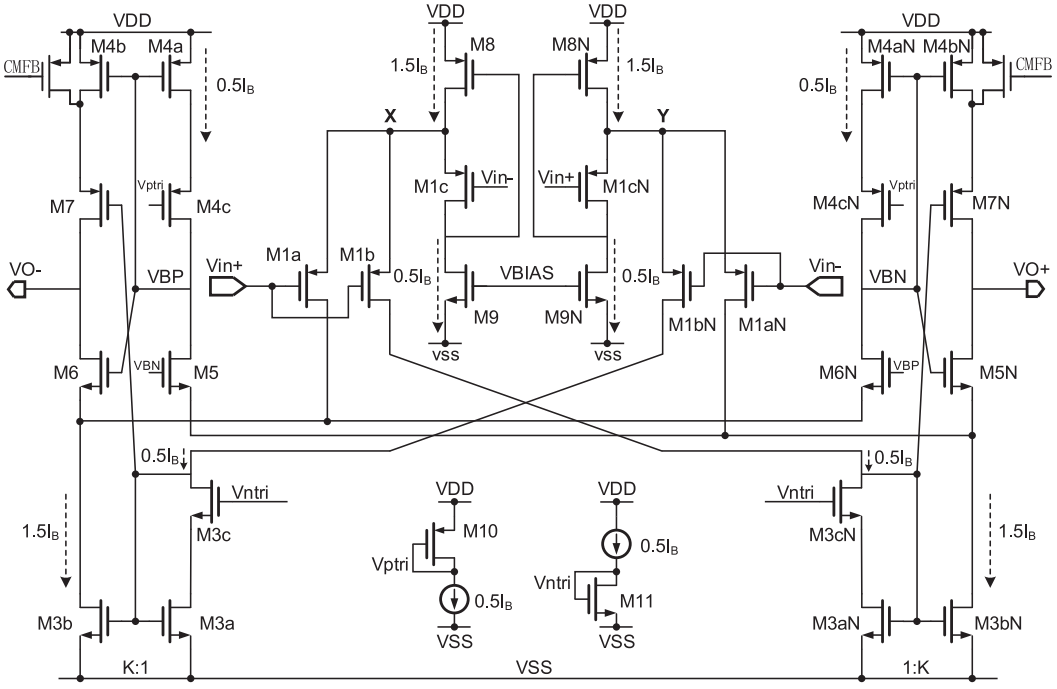

Fig. 2. The schematic of enhanced symmetric recycling OTA.