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Study of capacitance nonlinearity in nano-scale multi-stage MOSFET-only sigma-delta modulators

Hamed Aminzadeh

Department of Electrical Engineering, Payame Noor University, 19395–3697 Tehran, Iran

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ABSTRACT

Digital integrated circuits (ICs) can be integrated in low-cost digital CMOS technologies with less number of masks than a mixed-signal CMOS technology. This property, however, limits the access to reliable analog components such as linear capacitors and linear inductors. Regardless of the CMOS process, sigma-delta (ΣΔ) modulation of analog signals can be fulfilled by using ordinary MOS devices as capacitors. Called as MOS capacitors (MOSCAPs), these elements illustrate nonlinear C-V characteristic, although the thin gate oxide layer results a high capacitance per unit area. In this article, we investigate the effect of MOS capacitance nonlinearity on the overall performance of discrete-time sigma-delta modulators. To this end, a behavioral-level model of a MOSFET-only switched-capacitor (SC) integrator is proposed, and enables characterizing the transfer behavior of MOSFET-only modulators. The proposed model is used to analyze the linearity and to select a suitable architecture for the modulator. It helps to decide proper structure of each MOSCAP depending on its significance on the output linearity. In virtue of the new model, behavioral-level simulation of a 1-V 12-bit 20MS/s MOSFET-only 2 + 2 sturdy MASH (SMASH) modulator matches well to circuit-level simulations in 90-nm digital CMOS technology. For a −1.4 dB, 19.7 kHz input and an oversampling ratio of 16, the modulator achieves over 72 dB signal-to-noise plus distortion ratio (SNDR), only 3 dB lower than a conventional design based on linear metal-insulator-metal (MIM) capacitors.

1. Introduction

Sigma-delta (ΣΔ) modulators are considered as the dominant solution for high-resolution analog-to-digital (ADC) conversion of low-frequency analog signals [1,2]. A single-loop ΣΔ modulator can be implemented simply by using low-voltage single-stage analog amplifier, few comparators and a number of analog switches and capacitors. It can achieve a high signal-to-quantization noise ratio (SQNR) when noise shaping technique is combined with the idea of oversampling [3]. In spite of these advantages, single-loop modulators suffer from degraded stability for high noise shaping orders. A high-resolution single-loop ΣΔ converter with moderate oversampling ratio may not therefore remain stable, unless multi-bit quantizers with sufficient resolution are used. MASH modulators employ a few single-loop modulators in a cascaded order, and distribute the required order of noise shaping among less complicated structures. They remain potentially stable for high levels of quantization noise, although coarse quantizers can be used within each loop [1]. To minimize the effect of quantization noise leakage in the digital domain, perfect matching between analog noise transfer function (NTF) and digital noise cancellation filter is, however, required [3]. This can be achieved by employing high accuracy components, i.e. high-gain amplifiers and perfectly matched analog components, in the form of a complicated and power-hungry structure. To alleviate the need for perfect matching between analog and digital filters, the architecture of the modulator can be altered such that no digital noise cancellation block is necessary. According to the idea of sturdy MASH (SMASH) topology, SMASH modulator perform the noise shaping via analog filtering only [4], and is rather insensitive to the modulator coefficients [5]. These converters can achieve analogous performance to MASH modulators using very relaxed analog components (in particular, very simple amplifiers with DC gain as low as 35 dB can be used! [5]). SMASH modulators are therefore compatible to nano-scale CMOS technologies where few MOS devices can be stacked. The decreased sensitivity of SMASH modulators to analog imperfections also reduces their dependence to MOS capacitance (MOSCAP) nonlinearity. We therefore choose the SMASH topology to implement the MOSFET-only modulator of this work.

Special circuit techniques facilitate integrating analog circuits among several digital blocks of standard CMOS technology. The required capacitors can be realized using equivalent gate-to-bulk capacitance of available MOSFETs. In contrast to interlayer metal-insulator-metal capacitors (MIMCAPs), MOSCAPs exhibit high capacitance per

E-mail address: haminzadeh@ieee.org.

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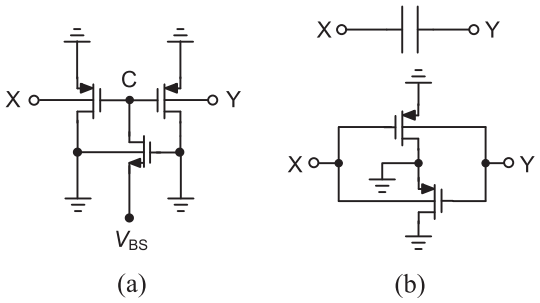

Fig. 1. Favorite solutions to implement MOS capacitors; (a) Series compensated depletion-mode (SCDM); (b) Parallel compensated depletion-mode (PCDM).

unit area and yield less parasitic to the substrate [6–10]. However, the application of these components is limited due to different charge distributions (and capacitance value) in accumulation, inversion, and depletion bias regions [6]. Analog compensation techniques, such as series, parallel (or combined [11]) improve the linearity of MOSCAPs [7]. The resulting capacitance will be very linear if the device is biased in accumulation or, possibly, in strong inversion. A high DC bias voltage is, however, needed for MOS devices in accumulation and strong inversion, leaving parallel compensated depletion-mode (PCDM) and series compensated depletion-mode (SCDM) MOSCAPs as practical choices in today's low-voltage nano-scale CMOS technologies [6–10]. A depletion-mode MOSCAP exhibits a balanced C-V behavior with improved linearity if it is realized in the form of a symmetric structure. Fig. 1 depicts two possible implementations when two *p*MOS devices are used within the signal path. The two devices are shunted together in the PCDM topology, and the gate and bulk junctions are connected symmetrically to the XY terminal, whereas the arrangement of the SCDM is such that the gate electrodes are tied together and their bulks are connected to the XY terminal. To avoid the chance of gate charging, a weak-inversion *n*MOS device also connects node *C* to analog ground via a constant bulk-source voltage (V_{BS}). A DC bias voltage in the order of +0.5 V increases reasonably the value of the resulting SCDM capacitance in 90-nm CMOS technology. This voltage increases the potential of the high-impedance node *C*, and can be generated using a regulated voltage supply [10], or a local bandgap Ref. [12]. Both implementations in Fig. 1 avoid the use of floating DC bias voltage with switching complications in nano-scale technologies.

To digitize the full-scale analog input with high accuracy, few single-loop MOSFET-only ΣΔ modulator topologies are reported in the literature [6,7,13]. None of these research works, however, studied the role of separate MOS capacitors on the modulator linearity. To quantify this effect on the performance of MOSFET-only modulators, this paper presents a comprehensive model for C-V characteristic of the internal MOSCAPs. The model was found very useful for analysis, and, correspondingly, digital calibration of MOSFET-only pipelined ADCs [8].

The same model is used in this article to analyze the behavior of the internal MOSFET-only integrators, and to extract the characteristics of multi-loop MOSFET-only modulators. It can predict, with high accuracy, the role of each MOSCAP on the overall linearity, and can be used for digital background calibration of the modulator [14,15].

The rest of this paper is organized as follows. In Section 2, the C-V characteristic of SCDM and PCDM capacitors are studied and the results are supported by circuit simulations in 90-nm digital CMOS technology. An analytic description of MOSFET-only switched-capacitor (SC) integrators is also developed and used to extract the transfer characteristic. The obtained transfer function is validated through circuit-level simulations in 90-nm CMOS process. Possible scenarios for implementing a 4th-order SMASH modulator using PCDM and SCDM capacitors are investigated in Section 3. To this end, the properties of the modulator are quantified in terms of linearity and area. Section 3 also presents the simulation results of different MOSFET-only modulators in 90-nm digital CMOS technology. The results are compared to conventional modulators implemented based on MIMCAP capacitors. The linearity of each modulator is measured in terms of the signal-to-noise-plus-distortion ratio (SNDR).

2. Analysis of MOSFET-only SC integrators

2.1. Characterization of MOS capacitors

Measurement results show that the C-V characteristic of SCDM and PCDM is symmetric around the vertical axis of C-V plane [7]. This is due to symmetric architecture of the MOSCAPs when viewed from the input terminal. As a result, odd-order terms of nonlinearity are highly suppressed and the capacitance value becomes an even function of the applied voltage. In general, we can describe the C-V dependence of the MOSCAPs illustrated in Fig. 1 as

$$C(V) = C_0(1 + mV^2 + nV^4 + ...), \quad (1)$$

where C_0 is the initial value of the MOSCAP for zero bias voltage, and the coefficients *m*, *n*, etc. are the factors of nonlinearity. These factors depend on the physics of the device along with capacitance configuration (i.e. PCDM, SCDM or combined), and are rather insensitive to absolute capacitance value. In practice, the factors higher than second

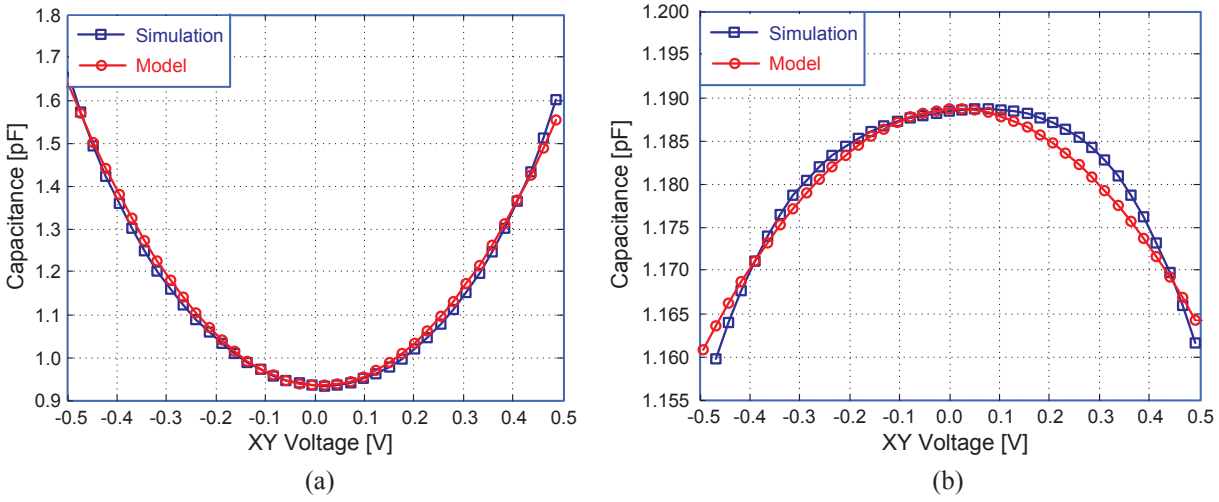

Fig. 2. Modeling the C-V characteristic of depletion-mode MOS capacitor in 90-nm CMOS. (a) PCDM (Avg. = 1.15 pF, W/L = 40 µm/20 µm, m = 2.8) (b) SCDM (Avg. = 1.18 pF, W/L = 60 µm/20 µm, m = −0.07, V_{BS} = 0.5 V).