Int. J. Electron. Commun. (AEÜ) 84 (2018) 74–83

Contents lists available at ScienceDirect

Int. J. Electron. Commun. (AEÜ)

journal homepage: www.elsevier.com/locate/aeue

Regular paper

Multi-phase low-noise digital ring oscillators with sub-gate-delay resolution

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ARTICLE INFO

Keywords:
Self-timed ring oscillators
Multi-phase oscillators
Coupled oscillators
Time resolution
Phase noise
Jitter

ABSTRACT

Multi-phase oscillators are often required to generate multiple clock phases with high frequency, high resolution and low-phase noise. This paper deals with self-timed ring oscillators (STROs), which are a promising solution for designing multi-phase clock generators. In STROs, the phase resolution can be adjusted as fin as desired by simply increasing its number of stages without frequency drop, and this resolution is not limited by the gate delay. In addition, different oscillation frequencies can be obtained by the same STRO depending on its initialization. Thanks to this configurability, $1/N$ $(-10{\cdot}log(N)dB)$ phase noise reduction is obtained at the cost of higher power consumption when the number of stages is increased N times, while keeping the same oscillation frequency. Moreover, clock jitter in STROs is reduced to the minimum and unavoidable component due to the white noise. Two test-chips have been designed and fabricated in STMicroelectonics CMOS 65 nm and in AMS 350 nm. Most of the measurements are perfectly in accordance with our theoretical claims.

1. Introduction

Oscillators are basic building blocks frequently needed in several applications. They are widely used for clock generation in communication systems, microprocessors and SoCs. In communication systems, a clear trend towards the use of high-speed serial links between RF transceivers and baseband digital signal processing circuits can be seen. This kind of links often requires generating a high frequency clock able to reach high performances in terms of timing jitter and phase noise. High frequency oscillators can be typically implemented using ring structures or LC circuits.

Multi-phase oscillators with high frequency are often required in communication systems. Although ring oscillators are relatively less efficient, in comparison to LC oscillators, in terms of phase noise and timing jitter performances, they are well-suited to generate multiple high frequency clock phases. They are composed of compact looped delay chains inherently multi-phase. Therefore, the design of low-phase noise low-jitter oscillators is crucial, especially when a large number of phases is required.

High frequency with fine phase resolution (tap-to-tap delay spacing between two successive phases) and multi-phase clocks are often required in many applications such as clock recovery systems [1] and in single chip testers [2]. Conventional inverter ring oscillators are often used to generate high speed multi-phase clocks due to their compactness and their simple structure. Nevertheless, their oscillation frequency is inversely proportional to the number of stages and their timing resolution is bounded by the propagation delay of one ring stage. Since the number of available phases is equal to the number of stages, the only way to obtain more output phases is to add more stages, which decreases the maximal frequency without improving the time resolution. In order to overcome this frequency drop with regards to the number of phases, several multipath ring oscillator schemes have been proposed to increase the maximal frequency of ring oscillators with multi-phase outputs [3–8].

Self-timed ring oscillators (STROs) are considered as a promising alternative for designing multi-phase clock generators due to their unique timing features. Different oscillation frequencies can be obtained by the same STRO depending on its initialization. In addition, STROs have also well-suited characteristics for managing process variability and offer an appropriate structure to limit the phase noise [9–14]. This paper deals with the design of multi-phase low-phase noise low-jitter clock based on self-timed ring oscillators. The novelty in STROs is that the phase resolution can be adjusted as fine as desired by simply increasing its number of stages without a frequency drop, and this resolution is not limited by the gate delay. In addition, $10{\cdot}log(N)dB$ phase noise reduction is obtained at the cost of higher power consumption

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https://doi.org/10.1016/j.aeue.2017.11.022
Received 5 September 2017; Accepted 23 November 2017
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when the number of stages is increased N times while keeping the same oscillation frequency. Moreover, thanks to the STRO stages characteristics, timing variations (jitter) of the clock provided by a STRO can be strongly attenuated. All these features are confirmed by simulations and measurement results.

The paper is structured as follows. Section 2 presents the background of multi-phase oscillators. Section 3 describes the self-timed ring architecture and its temporal behavior. Section 4 details the phase noise and jitter analysis of the STRO. The implementation and the experimental results are reported in Section 4. Finally, Section 5 states the paper conclusions and future works.

2. Multi-phase ring oscillators background

The simplest way to generate a multi-phase clock is the use of a looped delay chain, commonly called single-ended ring oscillator (Fig. 1(a)), which is inherently multi-phase. Each delay stage provides a π/N_d phase shift, where N_d is the number of delays, the remaining phase shift is provided by a DC inversion [15]. An odd number of stages is mandatory to maintain the oscillation in the case of a single-ended RO. Differential inverters are also used to reduce the conversion of power supply fluctuations and substrate noise to the phase noise, and to generate a complementary clock [16]. In fact, oscillators with in-phase and quadrature (I/Q) output signals are crucial in many applications. The generation of signals in quadrature requires ring-based inverters with an even number of stages. Many works deal with this subject [16–22]. In this case, the ring can have an even number of stages if the feedback lines are swapped. The oscillation frequency is the inverse of twice the sum of the individual delays t_d of all the stages, it can be expressed by (1) when the ring stages are identical.

$$F_{RO} = \frac{1}{2 \cdot N_d \cdot t_d} \tag{1}$$

In the conventional ring oscillators, according to (1), the oscillation frequency is inversely proportional to the number of stages. In addition, the timing resolution (tap-to-tap delay spacing between two successive phases) is bounded by the propagation delay of one ring stage. Since the number of available phases is equal to the number of stages, the only way to obtain more output phases is to add more stages, which decreases the maximal frequency without improving the time resolution. High frequencies with high phase resolutions multi-phase clocks are required in many applications.

In order to overcome this frequency drop according to the number of phases and/or to increase the time resolution, multi-path ring oscillators (MPROs) schemes have been proposed (Fig. 1(b)). A multiple-feedback-loop differential ring architecture has been proposed using three stage and four-stage designs. 55% speed improvement has been obtained for four-stage triple-feedback-loop compared to the three stage single-feedback-loop has been reported in [4] at its maximal operating frequency. In [5], sub-feedback loop topology has been introduced using interpolating inverter stages to construct fast sub-feedback loops for long chain rings to obtain both multi-phase outputs with higher frequency operation. The resulting operating frequencies are improved by over a factor of 2 in the best cases compared to the conventional RO. Negative delay skew schemes is used to reduce the minimal delay per stage below one stage delay [6]. It is based on cell delay smaller than a conventional inverter delay by inserting conceptual negative delay element at the input of one of the two transistors of the CMOS inverter. The resulting operating frequencies are 50% higher than those obtainable from the conventional approaches. A dual-delay path technique has also been adopted in the ring oscillator to obtain higher frequencies and to increase the tuning range [7] combining the normal delay paths with the negative skewed delay paths in the same ring oscillator. In [8], a multi-path structure has been proposed. A 47-stage penta-path stages ring oscillator is used to achieve a fine time resolution in a time-to-digital converter. To improve the effective resolution by a factor of 5 compared to classical inverter rings, the prototype presented in [8] uses a 47-stage penta-path gated ring oscillator. The problem that we face with the MPROs is the existence of different possible oscillation modes in the same ring with different frequencies, phase shift, and phase noise versus power tradeoff, which requires careful calibration and optimization in order to determine the dominant oscillation mode [3].

Coupled oscillators have been introduced to produce precise delays with subgate-delay resolution by exploiting the phase difference between events propagating in different rings running at the same frequency [23]. A two-input inverting delay stages are used to couple a number of identical oscillators. It is theoretically possible to obtain any number of phases by coupling more and more oscillators. In addition, they have the advantage of reduced phase noise: N coupled oscillators have N times less phase noise than a single oscillator [24,25]. Different architectures of coupled oscillators has been proposed and cited in [25,26]. To achieve the $1/N$ the near-carrier phase noise reduction, the coupling phase have to be chosen properly.

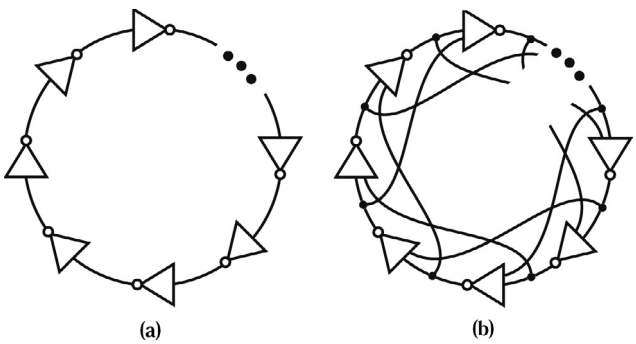


Fig. 1. (a) Single-path RO (b) multi-path RO concept [8].

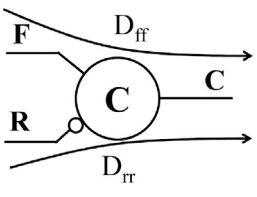
3. Self-timed ring oscillators

3.1. Architecture and behavior

A self-timed ring oscillator (STRO) is a looped control circuit of a micropipeline, as proposed by [27]. The ring stage, shown in Fig. 2(a), is composed by a C-element (Muller gate) and an inverter. The C-element is the basic element in asynchronous circuit design, introduced by D. E. Muller [28]. C-elements set their output to the input values if their inputs are equal and hold their output otherwise ($C = A \cdot B + C^{-1}(A + B)$). The truth tables of the C-element and the STRO stage are depicted in Fig. 2(b).

Fig. 3 shows the STRO architecture. Each stage has two inputs, one (F_i) is forwarded from the output of the previous stage (C_{i-1}) and the other one (R_i) is connected to the output of the next stage (C_{i+1}). F_i signals represent the request paths while R_i signals represent the acknowledgement paths.

In this architecture, several events can simultaneously propagate



STRO Stage				
F	R	C-element		
		A	B	C
0	0	0	1	C^{-1}
0	1	0	0	0
1	0	1	1	1
1	1	1	0	C^{-1}

(a) (b)

Fig. 2. (a) Symbol and (b) truth table of C-element and STRO stage.

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