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A novel miniaturized power amplifier with *n*th harmonic suppression

M. Hayati [a,b,*], S. Roshani [a]

[a] Electrical Engineering Department, Faculty of Engineering, Razi University, Tagh-E-Bostan, Kermanshah 67149, Iran
[b] Computational Intelligence Research Centre, Razi University, Tagh-E-Bostan, Kermanshah 67149, Iran

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ABSTRACT

In this paper, a novel miniaturized power amplifier (PA) matched by two proposed low pass filters (LPFs) with *n*th harmonics suppression is presented. In the proposed PA, the LPFs are employed as an output and input impedance transformer networks, which transform 50 Ω to the desired impedances. In the proposed PA the conventional output and input matching networks are eliminated, which results in 52% size reduction and 6% power added efficiency (PAE) improvement compared with the conventional PA. Moreover, using the LPFs at the output and input impressively suppress the unwanted harmonics (2nd–6th) with high level of attenuation. The proposed PA works at the 2.6 GHz, which is suitable for long term evolution (LTE) applications. The measured and simulated results are in the good agreement, which confirm the validity of the proposed method.

1. Introduction

With the demand of high-speed data communication, the 4th generation (4G), LTE system has attracted a lot of attentions. For LTE applications, power amplifiers (PAs) should be low cost, high integrated and light weight [1]. Nowadays, the growing demand for higher data rates and the increasing number of wireless communications users have resulted into rapidly rising power consumption. The energy efficiency of base stations should be constantly improved in order to reduce the power loss. Significant energy saving can be achieved by improving the efficiency of the power amplifier (PA) of RF transmitters used in the base station [2]. Different techniques have been proposed to increase the efficiency of power amplifiers. Envelope elimination and restoration (EER) [3], envelope tracking (ET) [4], Doherty amplifiers [5,6] and varactor-based dynamic load modulation [7] are the most common techniques being proposed to enhance the efficiency of PAs.

Power amplifier performances significantly depend on their output matching networks (OMNs). Nowadays, extensive researches have been performed on the OMNs to improve harmonic suppression [8,9], PA's efficiency improvement [10], bandwidth enhancement [11], multiband capability, etc. The OMN and input matching network (IMN) in the conventional PA occupy a large size, and they have several discontinuities between the narrow and wide lines, which excite high order modes [1].

In [8,9], to enhance PAE and suppress unwanted harmonics, filters have been used in the PA structure, but in these works, there is not any size reduction and OMN is still an indispensable part. In [1] BPF is used as the OMN, which results in 21% size reduction compared to the conventional PA and suppresses the 2nd harmonic, but the miniaturization and harmonic suppression in this work are not so prominent.

In the proposed structure, a miniaturized power amplifier integrated by two low pass filters (LPFs) at input and output is proposed. The applied LPF in this structure is based on a proposed filter in [12]. It works as an IMN and OMN, therefore, the conventional output and input matching networks are eliminated, which results in ultra size reduction and high harmonics suppression. Compared with reported works, the proposed PA demonstrates better size reduction (52%) and suppresses the 2nd–6th harmonics with high level of attenuation.

2. Design process

The schematic structures of the conventional PA, is shown in Fig. 1. In the conventional PA, the output and input matching networks occupied a large size, and they have several discontinuities between the narrow and wide lines. The OMN and IMN are used to transform 50 Ω to the desired impedances, which shown as Z_L and Z_S in Fig. 1.

The proposed PA is designed using a MW6S004N LDMOS transistor. The applied transistor is designed for class A or class AB base

* Corresponding author at: Electrical Engineering Department, Faculty of Engineering, Razi University, Tagh-E-Bostan, Kermanshah 67149, Iran.
Tel.: +98 9188312041.
E-mail addresses: mohsen_hayati@yahoo.com, hayati@razi.ac.ir (M. Hayati).

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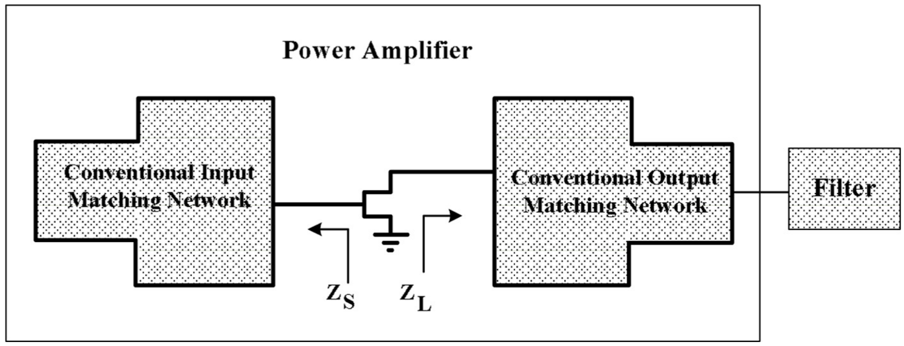

Fig. 1. Schematic diagram of the conventional power amplifier, with conventional IMN, OMN.

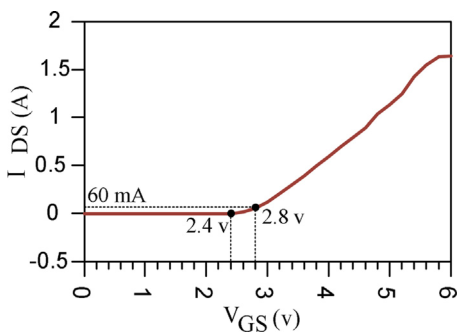

Fig. 2. Transfer characteristics of the applied device.

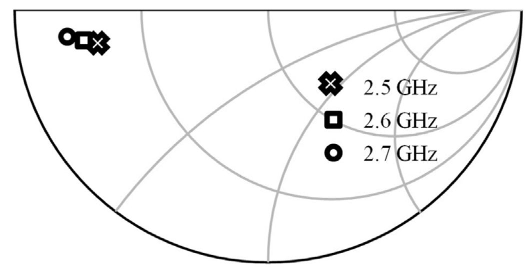

Fig. 4. Simulated optimum source impedances (Z_S) of the main device at 2.5–2.7 GHz frequency range.

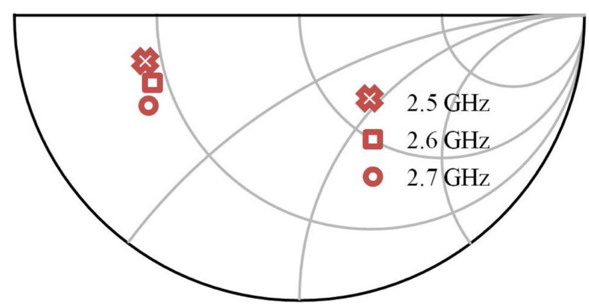

Fig. 5. Simulated optimum load impedances (Z_L) of the main device at 2.5–2.7 GHz frequency range.

station applications with frequency up to 2 GHz. Typical output power is 4 W, I_{DQ} = 50 mA and V_{ds} = 28 V.

The transfer characteristics of the applied LDMOS transistor MW6S004N, which performed with the Advanced Design System (ADS) software (Agilent Technologies, Santa Clara, CA) is shown in Fig. 2. The plot represents the range of gate voltages and the corresponding mode of operation with a drain voltage of 28 V. The amplifier is biased in class AB (quiescent drain current of 60 mA and gate voltage of 2.8 V). Increasing of the quiescent current resulted in better performances, but caused extra heating, so in the proposed design the current did not increase very much and there is a good trade of between heating and performances. Fig. 3 shows the output characteristics of the applied device.

3. Load/source pull

The first step to design the PA is to perform load/source pull simulation to find the optimum load/source impedances at the desired frequency (2.6 GHz). The load/source-pull simulations for the PA are performed with the Advanced Design System (ADS) software (Agilent Technologies, Santa Clara, CA) and resulting optimum load/source impedances at 2.5–2.7 GHz frequency range are shown in Figs. 4 and 5, while these values of the optimum load and source impedances are listed in Table 1. The optimum load and source impedances at the 2.6 GHz (desired frequency) are 12–14j Ω (Z_L) and 7.5–12j Ω (Z_S), respectively.

The PA parameters have been inferred from the dc *I*–*V* curves of the device (Figs. 2 and 3), and load/source pull analysis (Figs. 4 and 5). The values of the design parameters and their symbols are listed in Table 2.

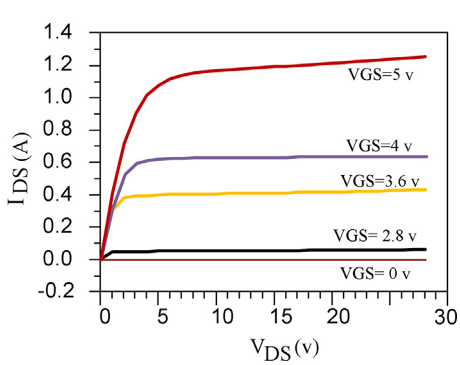

Fig. 3. Output characteristics of the applied device.

4. Proposed PA design and implementation

The schematic diagram of the proposed PA is shown in Fig. 6. As mentioned above the LPFs have a significant role in the proposed

Table 1
The optimum impedance values from load/source pull simulation in desired frequency.

Frequency	2.5 GHz	2.6 GHz	2.7 GHz
Optimum load impedance (Z_L)	11–12j Ω	12–14j Ω	11–16j Ω
Optimum source impedance (Z_S)	8–13j Ω	7.5–12j Ω	7–11j Ω