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Designing ternary quantum-dot cellular automata logic circuits based upon an alternative model☆

Saman Mohammadi Mohaghegh[a], Reza Sabbaghi-Nadooshan[b,c,*], Majid Mohammadi[d]

[a] Department of Electrical Engineering, Arak Branch, Islamic Azad University, P. O. Box 38135-567, Arak, Iran
[b] Department of Electrical Engineering, Central Tehran Branch, Islamic Azad University, Tehran, Iran
[c] School of Computer Science, Institute for Research in Fundamental Sciences (IPM), P. O. Box 19395-5746, Tehran, Iran
[d] Computer Engineering Department of Shahid Bahonar University of Kerman, Kerman 76137, Iran

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ABSTRACT

Three-valued logic is recently being considered in the field of multi-valued logic due to its competitive advantages over binary logic for development of state-of-the-art digital systems. Despite several advances in this area, a comprehensive model that could have a profound impact on the trend of such a newfound system has so far not been proposed. Therefore, this study is an attempt to design basic ternary Quantum-dot Cellular Automata logic gates and various combinational ternary circuits like adders by use of our proposed model. To verify the design circuits, proposed ternary logic circuits are simulated by newly designed TQCAsim software while to scrutinize the effectiveness of simulation method, some prior proposed conventional gates have also been simulated. Moreover, effective factors such as area, energy consumption, fault tolerant and cost are investigated in the proposed circuits. The results show that, in addition to proper characterization, designed circuits are conveniently applicable for digital systems.

1. Introduction

According to Gordon Moore's law, every 18 months the number of transistors that could be integrated into a single chip is doubled which results in saving space and minimizing device sizes. The limitations of CMOS technology scaling caused by heat generation affect the device speed and density. This calls for alternative technologies to develop such as quantum-dot cellular automata (QCA), single electron tunneling, molecular electronics, silicon nanowire, carbon nanotube, tunneling phase logic, resonant tunneling devices, spin transistors and superconducting electronics.

In QCA which first proposed by [1], information can be transferred from one cell to another by propagating a polarization state instead of electrical current. Owing to beneficial properties like small size, high packing densities, small signal delays and low power consumption, QCA has gained attention recently. It was first proposed in binary form, though, there are more than two truth values known as multi-valued logic (MVL), that provides fast performance and inputs/outputs reduction [2]. Among the MVL logics, ternary logic (tQCA) is the most practical one. More details on QCA and tQCA will be presented in further sections.

Recently, some studies have been introduced various models for ternary logic gates. The first model [3], focusing on ternary majority gates. Within this study, ternary AND and OR logic functions are implemented as a hierarchy of three majority gate structures. In the second model, adiabatic pipelining technique is suggested [4,5]. They proposed that using this technique can meet

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* Corresponding author at: Department of Electrical Engineering, Central Tehran Branch, Islamic Azad University, Tehran, Iran.
E-mail address: r_sabbaghi@iauctb.ac.ir (R. Sabbaghi-Nadooshan).

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the challenges in designing ternary logic gates. In fact, exploiting this model, wire, fan-out, inverter and majority gate architectures are introduced. In a later study, a ternary memorizing cell has been designed using the same model [6]. The third model [7], illustrated a method to design an optimal tQCA logic circuit which can calculate an arbitrary ternary logic function and still others [8] introduced their work which is inspired by [1] whose configuration consists of nine dots potential well instead of eight dots. They also suggested 3-input, nine dot potential well majority gate. The last model [9] puts forward nonconventional QCA cell which implements multi-valued logic circuits with irregular shapes for ternary cells.

In our earlier work reported in [10], we proposed a new model to design ternary logic gates. To examine the effectiveness of this model, some prior proposed conventional gates like Min and Max gates has been implemented. Moreover, all presented gates are simulated by newly designed TQCAsim software which is designed based on the proposed model. However, the aim of this paper is to design more complicated and combinational ternary circuits like adders. For this purpose, we design various ternary gates like different kinds of inverters, decoder, and cycle. Using these gates leads us to design adder and subtractor. The simulation results show that the proposed design circuits are applicable.

The rest of the paper is organized as follows: Background of binary and ternary QCA is described in Section 2. Section 3 proposes ternary logic design and Section 4 implements basic ternary gates. Section 5 describes some combinational ternary circuits and the related simulation results. Finally, Section 6 concludes the paper.

2. Background of binary and ternary QCA

The binary quantum-dot cell is a square-shaped cell with four quantum dots occupying the four apexes of the cell. Based on Coulomb repulsion law two electrons can only occupy antipodal sides in the cell. Hence, each cell can have polarization state of either $P = 1$ or $P = -1$ with binary value states 1 and 0, respectively. Unlike binary area, in MVL, each bit can take more than a single logic value and more data can be saved in MVL memories compared to binary one. Low cost and faster numerical analysis are other advantages of MVL circuits. A significant discussion related to MVL is ternary logic [3] which can accept the values ``true", ``false", and ``unknown" (e.g. Łukasiewicz's, Kleene's and Priest's "logic). Ternary logic equals binary logic and even surpasses it, in some aspects. Ternary logic has main advantages which are as follows: (i) the least complex logic among MVLs (simplicity); (ii) ability to store more information in comparison with conventional binary logic; (iii) high speed; (iv) high performance and (v) cost-effective design. Therefore, using this logic can be beneficial in modern computing devices.

It is worth noting, one of the effective three-valued logic systems that can be compared with balanced ternary is Kleene's logic. The basic logic gates such as min (and), max (or) and inverter (not) gates are identical in Kleene's logic and balanced ternary logic. Naturally, all the ternary circuits are implemented by use of these basic gates and hence, the results of our proposed circuits are valid in Kleene's logic too. More information about this logic can be found in [11].

The most well-known ternary quantum-dot cell encompasses eight quantum wells located in a circle shape and a pair of electrons that can tunnel conveniently between these wells. Based on Coulomb Repulsion Force, a pair of electrons always stays furthest away from each other. Due to cell structure, these electrons can be placed in four different positions. Each position is equivalent to one logical state such as -1, $+1$, 0, and 0 (balanced ternary) or 0, 1, ½, ½ or 0, 0, 1, 2 (unbalanced ternary). Note that, two different positions have the same value. The electrons are allowed to move in a single cell, therefore, there is neither electron transfer between neighbor QCA cells, hence, current flows from one cell to another.

As mentioned so far, two mobile electrons are present in each QCA cell. Practically, these electrons can settle in their positions in quantum dots by means of the clock signal that fed to the input of QCA circuit. In fact, the clock can provide power and controls the movement of electrons within a specific cell (data transmission control). When the information is transferred to the circuit, it is joined with other inputs and produces the desired output. However, delayed inputs prevent the dissemination of information. Consequently, clock creates synchronicity in different parts of the circuit. It should be noted that QCA circuits do not need any external power. In any standard CMOS, the clock has two phases, but in QCA, it consists of four, including hold, release, relax, and switch. In other words, one of the clock roles is to control and change the polarization of the cell. Initially, cells are unpolarized, when the cell is biased by the input voltage (clock voltage), the barriers begin to rise during the switch phase and the movement of electrons is prevented, hence, electrons movement becomes slow. In hold phase, the barriers are raised completely and electrons remain in their own positions. In release phase, the barriers are lowered, then, electrons are released slowly while in relax phase, the barriers remain lowered and electrons are not localized to any particular dots within the cell, however, they are still confined to the cell and as a consequence, cells are unpolarized. More information about the clock performance can be found in [12].

It should be noted that, up to now, some binary QCA designs based on the various fabrication methods are theoretically and experimentally investigated [13,14]. However, according to our knowledge, no specific experimental results of ternary QCA have been reported.

3. Proposed ternary logic design

The main aim of this paper is to design various ternary logic circuits based on our earlier model reported in [10]. In this work, first, basic ternary logic gates like ternary majority gate and some ternary inverters are designed. Using this basic gates leads us to design combinational ternary circuits. Then, to evaluate our findings and results, all the proposed circuits are simulated precisely by TQCAsim software, designed for the first time by our team at IAUCTB laboratory. In addition, a trial version of TQCAsim software can be found online [15].

Before beginning to design, some significant items should be mentioned. The first item is cell configuration and value. Fig. 1,