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Design of multiple-valued logic gates using gate-diffusion input for image processing applications☆

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ABSTRACT

In this work, unique characteristics of carbon nano-tube field effect transistor (CNTFET) are used to propose a universal cell with a simple architecture based on the binary modified gate-diffusion input (m-GDI) method for designing fundamental gates in the voltage-mode multiple-valued logic (MVL) with any arbitrary number of logic levels for processing at nano-scales. The results of the simulations confirm more energy-efficiency, larger noise margins and lower sensitivity of the proposed designs in different logic levels as compared with the state-of-the-art designs. The effects of the process, voltage and temperature (PVT) variations are extensively evaluated by Monte–Carlo simulation. According to the results, the proposed designs are robust against PVT variations and noise. The proposed structure is applied to the MVL-based image processing. The results show that the output images of the proposed MVL-based inexact gates have an appropriate quality in compare with the images generated by the other similar exact gates.

1. Introduction

The high chip area creates limitations for the configuration of binary (two-valued) circuits [1]. In order to dominate the difficulties, the logic with more than two values with limited or unlimited logic levels like multiple-valued logic (MVL) [2] or fuzzy logic are used instead of the binary logic. MVL system has better characteristics, such as better process ability, more data processing and store capabilities per unit area and connection complexity as a result of lower number of active components [1] and higher density of packaging [3], in compare with the conventional binary systems. By using MVL system not only the performance is increased, but also the power consumption is reduced as the number of internal connection capacitor is decreased [4]. Carbon nano-tube (CNT) field effect transistor (CNTFET) seems to be very promising for overcoming the mentioned problems that the conventional silicon metal-oxide-semiconductor field-effect transistor (Si-MOSFET) is facing in designing MVL circuits. This is due to the fact that the most prevalent and suitable method for designing voltage-mode MVL circuits is the multiple-V_{th} (threshold voltage) design technique and the desired V_{th} can be obtained by adopting proper diameter for the nano-tubes (D_{CNT}) of the CNTFET device [5]. In this paper first, the implementation of binary inverter gate cells with unbalanced and balanced voltage transfer characteristic (VTC) curves is presented. The inverter gates are designed by the binary modified gate-diffusion input (m-GDI) method [6,7] based on basic GDI technique [8]. This method is useful for designing the low-power fundamental logic gates through employing CNTFETs [6]. After that, the advantages of the efficient performance of the m-GDI method in designing the logic gates [6], flip-flops [9] and static binary and ternary (three-valued) memory cells in nano-process [7,10–11] are presented. In addition the evaluation parameters of the other

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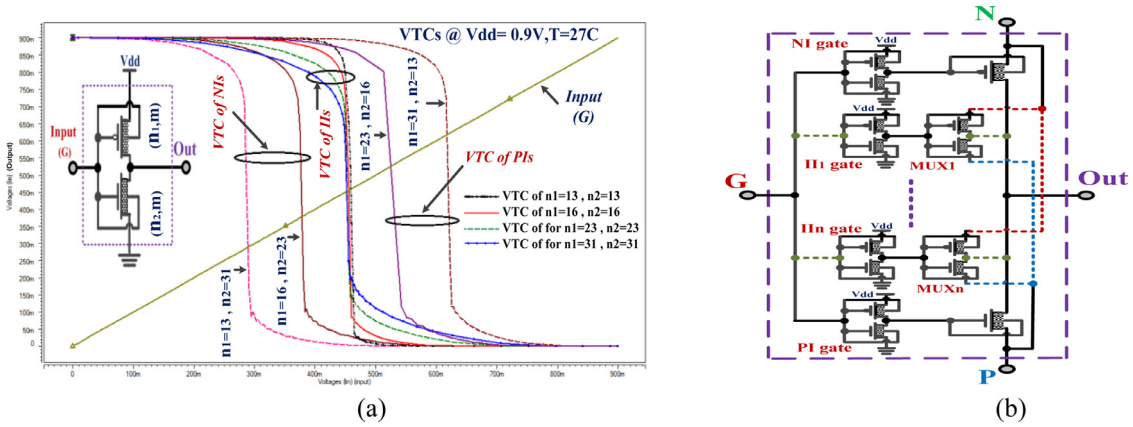

Fig. 1. (a) The general binary inverter cell and its VTC curves. (b) The proposed universal GDI cell structure.

designed circuits based on m-GDI cell can be optimized with the algorithm [10,12]. In addition, the novel universal GDI cell structure using inverter gate cells based on binary m-GDI method is proposed. This structure is used for designing fundamental logic gates with full swing output in the voltage-mode MVL with any arbitrary number of logic levels for nano-electronic circuits. The focus of the work is on the challenges existed in designing fundamental logic gates in different logic levels such as: ternary, quaternary (four-valued) and penternary (five-valued) that are implemented based on proposed universal structure in nano scale. The impact of process (such as number of CNTs), voltage and temperature (PVT) variations are analysed with Monte–Carlo simulation. The results show that the implementation of logic gate cells based on the proposed universal structure has dramatically lower power consumption, larger noise margins and lower sensitivity to process with substantial small standard deviation (Std. Dev.) compared with other state-of-the art designs in same technology. Also the proposed universal structure is applied in image processing. The results show that the inexact fundamental logic gates based on the proposed universal cell provide excellent capabilities to accomplish logic functions on the images with respect to peak signal-to-noise ratio (PSNR) more than 50 decibel (dB) in comparison with the exact fundamental logic gates, thus it is totally acceptable for most of the similar applications. The paper is organized as follows: The proposed universal GDI cell is presented in Section 2, the fundamental gate circuits in different logic levels based on the proposed universal cell are proposed in Section 3. Simulation results, analysis and comparisons are presented in Section 4. The application of the universal GDI cell in image processing is described in Section 5. Finally the whole work is concluded in Section 6.

2. The proposed universal GDI cell structure based on the binary m-GDI cell

Fig. 1 shows the general state of the implementation of an inverter gate cell with a view to Table 1 and its VTC curves based on binary m-GDI technique [6], where n_1 and n_2, respectively, are the indexes for pull-up transistor network P-type CNTFET (P-CNTFET) and pull-down network N-type CNTFET (N-CNTFET) in the general m-GDI cell with the common index $m = 0$ for two transistor networks. According to Fig. 1(a), with different choices of n_1 and n_2 indexes (number of nano-tubes for two transistor networks) in three types of binary inverter: negative inverter (NI) gate and positive inverter (PI) gate (with unbalanced VTC curves), intermediate inverter (II) gate (with balanced VTC curves) can be achieved. With a view to Fig. 1(a), in order to implement binary inverter gates, high-V_{th} N-CNTFET and low-V_{th} P-CNTFET are utilized for implementing PI gate ($n_1 > n_2$), low-V_{th} N-CNTFET and high-V_{th} P-CNTFET are used for implementing NI gate ($n_1 < n_2$) and same-V_{th} for N-CNTFET and P-CNTFET are utilized for implementing II gate ($n_1 = n_2$). Using the general inverter cells based on binary m-GDI method, the basic universal GDI cell structure for voltage-mode MVL designs is presented and shown in Fig. 1(b). According to Fig. 1(b), body of the universal GDI cell is configured with inserted binary inverters with NI and PI gate cells in the common input (G) of the basic binary m-GDI cell and also by replacing P and N diffusion terminals related to the presented binary m-GDI cell of [6]. In the body of the proposed universal GDI cell for creating more levels, one branch of II gates that are series with binary multiplexer (Mux) (with a view to Table 1) should be inserted between the main input and output terminals. P and N terminals of the binary Mux gate, which is inserted in each branch, should be connected to N and P terminals of the universal cell structure, respectively.

Great advantage of the proposed cell is its expandability for designing MVL circuits with any arbitrary number of logic levels by

Table 1
The producing of combinational logic gates with the m-GDI cell.

N	P	G	Out	Functions
'1'	**B**	**A**	$A + B$	**OR**
B	**'0'**	**A**	$A.B$	**AND**
C	**B**	**A**	$\overline{A}B + AC$	**Multiplexer (Mux.)**
'0'	**'1'**	**A**	$\overline{A}$	**Inverter (NOT)**