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High-Speed Virtual Logic Network on Chip Router Architecture for Various Topologies☆

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ABSTRACT

Due to numerous complex routing links, traffic congestion and latency becomes an important issue in advanced Network on Chip (NoC) architectures. For this, we propose High-Speed Virtual Logic Network on Chip router architecture (HSVLN) for controlling the traffic congestion and deadlock issues, and High-Speed Routing Algorithm (HSRA) that can reduce the latency by selecting the minimal interval paths. When we analyze the HSVLN for various topologies, its performance seems to be 50% better than existing router architectures. In reality, HSRA incorporates with HSVLN and it is examined with all proposed topologies such as the 2D-Global Mesh over Local Mesh (GMoLM), 3D-Mesh and 3D-Torus. Simulation and synthesis results of HSRA carried out by using Xilinx 14.7 and targeted on the Vertex-7 FPGA. We have analyzed the performance of HSRA for all proposed topologies, and their results are manifested by measuring with respect to latency and throughput. 2D-GMoLM showing an average reduction of latency by 3/5 times, enlarging the area by 1/4 and an increase in throughput by 1/3 times compared with 3D-Mesh and 3D-Torus. Therefore, when we compared with other two topologies, HSRA showed an adequate performance in 2D-GMoLM.

1. Introduction

Network on chip (NoC) is a unique approach in Multiprocessor System on Chip (MPSoC) applications. It has four significant devices, such as Router, Network Interface (NI), routing algorithm and IP cores. A typical model of 3×3 NoC [1] is illustrated in Fig. 1.

In reality, designing the vital component of router architecture is one of the significant challenge in NoC. Each router connects with one IP core and also connected to one or more neighboring routers [2]. The router performs a vital role because it controls the traffic congestion and also deadlocks in the cumbersome network.

Existing Wormhole and Virtual channel router architectures are limited to five directions, such as east, west, north, south, and local ports. Each input port has one buffer and it holds the packets temporarily until the output channel is busy. The input queue buffer-less router also known as Wormhole router. A set of multiple buffers (Virtual memory) available on each input port of a router which is considered as a Virtual Channel Router (VC) router [3,4].

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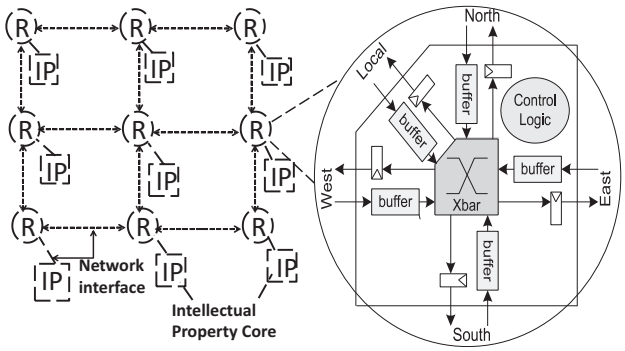

Fig. 1. Network on Chip.

Though the VC router increase the throughput, but it occupies more area and consumes more power. A single input queue buffer-less router can reduce the area, but its performance is poor. Each and every packet is allowed one after another in buffer-less router because of the single input queue buffering system. So, the buffer-less router will not be allowed a new packet until it completes the process of previous packet delivery [5]. Hence, this type of approach may not control the traffic congestion as well as deadlock problems. Even in the VC router, there is a problem with starvation because of no priority mechanism to transport the packets [6].

The next challenge in NoC is a Network Interface (NI) and it is interconnected between router to router and router to Intellectual Property (IP) core. It is to be noted that, IP cores are reusable cores, viz, memory, processor, crypto core, and so on.

The pivotal significance in NoC is a routing algorithm. In general, any routing algorithm provides the instructions to route the packet as well as it schedules the time period for transmission of packets in a huge network. Lets suppose the time allocation is inadequate, and which might lead to the problems like congestion, contention, starvation, latency and so on in the system. Allocation of the time period is the most tedious job for large NoC. Hence, the performance of the router, NI, and routing algorithms are considered as substantial challenges in NoC.

The main objectives of this paper are as follows

- A priority-based system is used to eliminate starvation issues and Look-Ahead routing method is employed to route the packets to the desired destination.
- HSRA and HSVLN proposed for reducing the latency, deadlock, and traffic congestion.
- To apply a sanity logic when critical congestion occurs.
- HSRA and HSVLN examined with different packet lengths for 2D-GMoLM and their performances compared with two other topologies in terms of throughput and latency.
- The performance of proposed router and existing virtual channel router where these two are compared and analyzed in terms of latency [6]. [Latency=((number of routers communicated * required number of cycles) – 1) + number of transmitted packets)].

In extension to our earlier publication in [7], we have made an improvement in routing algorithm and a slight change in the router design. Even though there is a cumbersome network in NoC, HSRA is able to select an optimized shortest-path and also can manage traffic congestion (with the help of HSVLN). A priority based mechanism can manage the starvation issues and also can handle the deadlocks in existing NoC router design using virtual storage mechanism.

The following sections are arranged as follows: Related work briefly described in Section 2. Application of the router design depicted in Section 3. An analysis of proposed routing algorithm explained in the Section 4. Implementation results presented in a Section 5. The final discussion deals with the conclusion.

2. Related work

Pasricha et al. [8] presented an automated synthesis of high-speed bus communication architecture implemented for NoC based MPSoC. This design has saved up to 2.1X to 3.1X components when compared to fully connected bus communication architecture.

Samman et al. [9] proposed a dead-lock free multicast routing for on-chip interconnections. An interesting notice point in the wormhole router architecture of on-chip, where the flits are allowing from various wormhole router and which are interleaved or multiplexed at a flit level on the same link. In this paper dead-lock issues are managed by using hold-release tagging mechanism.

Vladimir et al. [10] designed a nice perception called an automatic synthesis method for hybrid NoC topologies. In this design, deadlock-free routing algorithm prevented the problem of congestion. Here in this approach every time the algorithm needs to vary based on the design complexity.

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