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Online placement and scheduling algorithm for reconfigurable cells in self-repairable field-programmable gate array systems☆

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ABSTRACT

Most of the high-end very-large-scale integration- (VLSI-) based systems use a field-programmable gate array (FPGA) as their core component. As the complexity of systems increases, the chances of fault occurrence also increase. For systems that are part of safety-critical and mission-critical applications, even a single fault can result in entire mission failure. Fault tolerance techniques need to be installed in such systems to ensure reliable, prolonged operation in spite of fault occurrence. The level of fault tolerance exhibited in nature is very remarkable. Scientists are trying to reach that level of fault tolerance in the electronics world as well, which is not always completely acquirable. Basically, fault tolerance in an FPGA is achieved by the use of spare modules, which leads to high area overheads and routing complexity. The higher the number of faults to be handled, the greater the number of spares that will be required. Partial reconfiguration has always been a proven technique to improve the efficiency and flexibility of FPGAs. This paper discusses a multiple-fault repair algorithm for FPGA-based reconfigurable systems, using dynamic runtime partial reconfiguration, in order to relocate faulty modules. Three variants or cases of repair using the algorithm are discussed and demonstrated, namely, placement with the best resource utilization, placement with the least routing overhead, and a case to generate continuous free space for the relocation of a faulty module. The main advantage of the algorithm is its flexibility, which means that it can be used according to user demands and system lifetime requirements. Maximum care is taken to eliminate chances of an unrepaired fault or a repair that degrades the performance of the system. The algorithm can handle multiple permanent faults with the best resource utilization and the least overheads. The performance of the algorithm is analyzed quantitatively, while a comparison is made with some previous studies in the literature to justify the algorithm efficiency.

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1. Introduction

Fault-tolerant systems were introduced in the 1990s, and have been an interesting area of research ever since. The complexity of systems has increased so much that reliability issues related to this have also exponentially increased. Most VLSI applications, which demand high computational capability, use FPGAs for implementing their designs. Applications in the systems of rockets, spacecraft, aeroplanes, missiles etc. utilize FPGAs to implement their central working unit. In such safety- and mission-critical applications, the system is expected to function under very adverse conditions of temperature and pressure. In space applications, the circuitry is continuously exposed to radiation from the sun and other cosmic sources. This can adversely affect the internal structures and configurations of FPGAs, which leads to unintended changes in the design implemented within the integrated circuits (ICs); this is referred to as a fault. Wear-out is also a major cause of defect in FPGAs in the long term. A defect normally affects a particular location within the ICs. It can be expressed at different levels of resolution, namely, fine grain or coarse grain. In the case of fine-grain resolution, the fault can be denoted as a faulty transistor or faulty configurable logic blocks (CLBs). In coarse-grain resolution, a fault can be said to affect a module, or the entire FPGA can be considered to be faulty. In either case, to repair a fault and to nullify its effect, it is essential to isolate the faulty module. Years back, if a chip within the central processing unit (CPU) of a computer became faulty, the entire CPU would undergo replacement, which led to the wastage of many healthy resources along with the faulty item. A more effective repair with less resource wastage can be done by the fine-grain isolation of the faulty module. Even after thorough and cautious manufacturing processes, many of the systems that are produced today contain faults, which are only revealed in the field during runtime. These systems, when introduced into the industry, create yield loss and can sometimes pose a threat to material and human life. Therefore, critical systems must always be designed and implemented with in-built fault-handling capabilities. Reconfigurable devices, such as FPGAs, provide potentially enhanced platforms for the implementation of such self-adaptive high-end systems.

Self-healing or self-repair is an idea that is basically inspired from the living world around us. The level of repair or the healing power exhibited by living beings cannot be fully gained in the silicon-based electronics world. But, efforts have been made by the research community to almost attain this level of fault tolerance, so that systems can work reliably until the end of a guaranteed lifetime. Therefore, most self-repairing techniques that are seen in the literature are algorithms or architectures, which are inspired by the living world around us. Commonly used fault-tolerance methods for FPGAs range from hardware redundancy techniques, such as triple modular redundancy (TMR) or dual modular redundancy), to online adaptive architectures. Basically, each of these methods attempts to completely repair or nullify the effect of a defect occurring within the system with the least overheads in terms of time, area and routing.

The self-repair algorithm discussed in this paper is for reconfigurable FPGA-based systems, which use modular reconfiguration to implement the intended design into the IC. Each module of different size and priority is considered and the repairing technique is chosen according to the priority of the infected cells. While most of the traditional methods use more spare cells to achieve higher fault coverage, the proposed algorithm uses a single spare and module relocation to repair multiple faults with the least area overheads. According to the application, each system may have different design specifications, e.g., some must be designed with the best resource utilization, while some require less area overheads or less routing overheads. To try and meet all these demands, three repair methodologies are included in the algorithm covering all these three aspects, namely, repair with the maximum number of faults without performance degradation, repair with the best resource utilization, and repair with the least routing complexity. The algorithm can be flexibly used by the designer according to system longevity and customer specification.

This paper is organized as follows, Section 2 discusses previous works in this research area, Section 3 discusses about the proposed work and introduces terminology used throughout this paper, Section 4 explains about the repair using faulty module relocation, Section 5 discusses the pseudo code of the proposed algorithm, Section 6 discusses the results and compares the area overheads, routing complexity, faulty coverage with some existing works, Section 7 summarizes the major points discussed in the research work.

2. Previous works

Methods to achieve fault tolerance in FPGAs have been an interesting area of research ever since they were introduced into the industry a few decades back. As most FPGA applications include high computational complexity, methods to maintain a reliable operation, even after a fault has occurred, are necessary [1]. Techniques that include hardware redundancy or bio-inspired algorithms are the most popular. TMR is one of the most widely used methods of fault tolerance in FPGAs [2]. It is a hardware redundancy method that uses three units working simultaneously, among which, two are replicas of the first unit, while the primary outputs from the three units are taken via a majority gate. This creates high area overheads, while being able to repair only a single fault (limited number of replicas). As the major disadvantage of TMR is area overheads, variants of TMR have also been proposed, such as partial TMR [3] or TMR with alternative computing [4].

Among the different methods of FPGA fault tolerance, the most efficient and flexible are those that utilize the reconfiguring property of the FPGA. Recent studies have pointed out that relocation of reconfigurable modules and defragmentation can considerably enhance the efficiency of reconfiguration [5]. Many self-repairing systems that have been proposed to date were designed by taking inspiration from biology [6]. Embryonics is the field of electronic systems, inspired by living organisms or, more specifically, the embryonic development of living organisms [7]. Every living organism is born with some

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