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An efficient design of Vedic multiplier using ripple carry adder in Quantum-dot Cellular Automata☆

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is one of the emerging nanotechnologies, which yields attractive features like high speed, low power consumption and smaller size for implementing computing architecture in contrast to the CMOS technology. Numerous studies of adders and multiplier have been reported in this direction using QCA. This paper mainly focuses on designing of 8×8 Vedic multiplier in QCA using Urdhva Tiryagbhyam sutra. An efficient structure of 4-bit Vedic multiplier is used to construct an 8-bit multiplier. Moreover, the additions of generated partial products are realized using ripple carry adders and full adders. A generalized structure of $N \times N$ Vedic multiplier and the complexity of $N \times N$ multiplier design is also discussed. All the designs are simulated on QCADesigner tool and it confirms the efficiency of the proposed design. The simulation results show that the proposed design of 8×8 Vedic multiplier has reduced 60% cell count, 78% area, and 75% delay as compared to the 8×8 Wallace multiplier. In addition, it achieves equal complexity in term of cell count, but delay and area are reduced by 64% and 18% respectively compared to Array I multiplier. Furthermore, a general expression for the number of majority gates, inverters, crossovers, and delay is derived and compared with the Array I and Array II multiplier.

1. Introduction

Complementary metal–oxide–semiconductor (CMOS) is an important class of integrated circuits. It is widely used in chips such as microcontrollers, microprocessors, RAM and other digital logic circuits because it has key features like low power operation, high density, and high speed. Further higher density and speed are achieved by the scaling. But nowadays, CMOS device is expected to reach its physical scaling limit. Due to this, CMOS technology leads to the problems like Gate leakage current, interconnection noise, design complexity and stray capacitances [1]. These problems limit the use of CMOS technology. To overcome these problems, the International Technology Roadmap for Semiconductors (ITRS) paved the way for future alternative technologies. QCA is one of the suitable solution, which provides a new and unique approach for logic computation at Nano-scale [2]. CMOS technology uses voltage levels for binary computation, whereas QCA uses free electron location in the QCA cell for logic evaluation [3]. So, QCA cell performs the key role in QCA technology and it is used for logic

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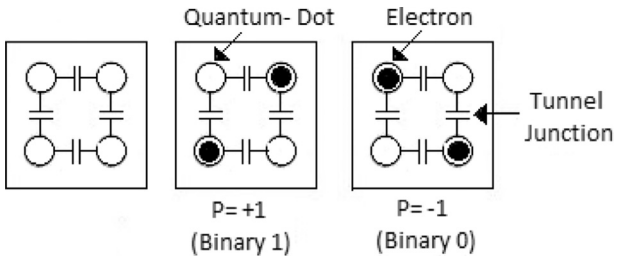

Fig. 1. Basic QCA cell with two possible polarizations.

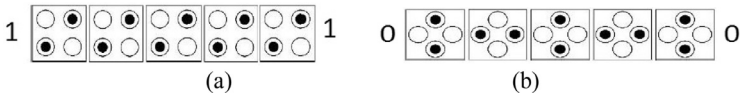

Fig. 2. QCA wire: (a) 90° wire: (b) 45° wire.

computation and interconnection, i.e. Data transmission [4]. Recent papers show that QCA circuits can achieve high density, fast switching speed and room temperature operation [4–6].

Recently, various designs of arithmetic operation in QCA have been reported, it includes the design of sequential circuits, ALU, shifter, comparator, adders, array divider, configurable logic block and array multipliers [7–18]. As multipliers are one of the essential component in most of the digital systems such as DSP, fractional order digital differentiator [19], and general purpose processors, having a high speed and less complex multiplier is significantly important. With the advancement of technology, a few new designs have been reported for the digital multipliers [12–14].

This paper mainly focuses on the design of 8×8 Vedic multiplier, developed using a 4×4 Vedic multiplier as the basic building block, which is efficient in terms of area, design and delay. In the existing 8×8 Vedic multiplier [11], the generated partial products are added by the three 8-bit ripple carry adders. In contrast, the proposed design uses only one 8-bit ripple carry adder, one 8-bit full adder (FA) and 3-bit ripple carry adder (using only half adder (HA)), which reduces both the area and delay of the multiplier architecture.

The rest of the paper is organized as follows: QCA terminology is explained in Section 2 and efficient design of 4×4 Vedic multiplier is presented in Section 3. The proposed 8×8 Vedic multiplier is explained in Section 4. The general structure for the $N \times N$ Vedic multiplier is reported in Section 5. The generalized expression for number of majority gates, inverters, crossovers and delay of *n*-bit Vedic multiplier are given in Section 6. Simulation results of the proposed design, analogy and complexity of the design are discussed in Section 7. The conclusions are given in Section 8.

2. Terminology

QCA Cell is the primary component of the QCA circuit design, which is shown in Fig. 1. It is a square-like structure with four quantum dots, which is fixed at the four corners of the cell. Quantum dot is nanometer size conducting material, which is surrounded by an insulating material. This type of arrangement in the quantum cell has the ability to trap the electrons in a third-dimensional quantum-dot and it cannot escape without enough electrical energy. All four quantum-dot are connected by four tunneling junctions and there are two free electrons, which have the ability to tunnel between quantum dots. Electrons repel each other due to the Coulomb force by which they attain two diagonal arrangement according to their polarization (P) or neighbor cell polarization [3]. These two arrangements have negative and positive polarities, which represent the binary value '0' and '1' respectively as shown in Fig. 1.

2.1. Basic QCA elements

In QCA, the primary Boolean logic function can be realized by the physical interaction between cells and additive nature of the coulomb force. The basic QCA logic device includes QCA wire, QCA Majority Gate and QCA Inverter as explained below.

2.1.1. QCA wire

QCA wire is realized by allocating QCA cells side by side in a series. In this type of arrangement, the next cell occupies the polarization from the previous cell because of physical interaction between the cells and also its polarity depends on the position of the cell. Fig. 2(a) shows 90° wire, and Fig. 2(b) shows 45° wire (dots are rotated by 45°).

2.1.2. QCA majority gate

QCA majority gate takes advantage of the additive nature of Coulomb forces as shown in Fig. 3 [3]. It requires 5 quantum cells where 3 are input cells, one is an intermediate cell, which gives the net force of the inputs and output is taken from

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