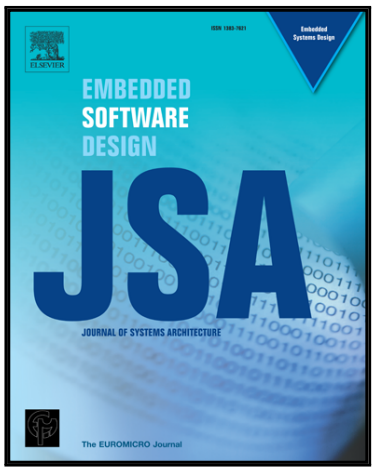

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Abstract

Technology scaling has enabled the integration of large number of transistors into a single chip, leading to performance enhancement via incorporation of Processing Elements (PEs), Intellectual Property (IP) cores and Memory Units together on the same platform. On the downside, it has led on-chip components to be more susceptible to faults, both permanent and transient. Permanent faults are predictable in nature and can be dealt with at the time of manufacturing or in field using spares/redundancy. Transient faults also adversely affect the application performance but are unpredictable in nature. Handling transient faults is a challenging task, especially in a real-time system where different applications are executed with various timing constraints. Although significant amount of work has been reported in literature for transient fault management, it lacks addressing the temporal constraint satisfaction of the tasks while restricting the energy expenditure of the system. Existing fault tolerant policies do task replication to ensure higher percentage of deadline satisfaction but at the cost of higher energy consumption. Checkpointing approach can make energy consumption low, however, the number of tasks satisfying their timing constraint also becomes low. Thus a fault tolerant policy which could jointly address the timing and energy constraint in a real time system is desirable. This work proposes an algorithm to intelligently perform a fault-tolerant resource allocation in real-time dynamic scenarios where tasks of applications are not known apriori. The slack times of the incoming tasks have been exploited in the application mapping/scheduling phase of the algorithm, to assign a fault tolerant policy to the corresponding task for mitigating the effect of transient faults. This helps to improve the deadline satisfaction of the task and also reduce the energy consumption. While comparing with existing works, the proposed algorithm achieves 19.8%, 43.5% and 85.8% improvement in deadline satisfaction compared to MXR[1], CPR[2] and TR[3], respectively. On an average, the energy consumption is reduced by 29.1% and 6.7%, compared to AR[4] and MXR[1].

Keywords: Network-on-Chip, Dynamic Mapping and Scheduling, Energy, Deadline, Fault tolerance.

1. Introduction

Advancement in deep sub-micron technology has increased the integration capacity of number of on-chip components such as Processing Elements (PEs), Memory Units and Intellectual Property cores and has helped to address the demand of high performance computing. Data transmission between these components is an important aspect as it affects the system performance. Transmission is affected by the communication backbone between PEs. The traditional shared bus-based and point-to-point technologies suffer from limitations in connecting these components. Network-on-Chip (NoC) has been proposed as a solution - an efficient and highly scalable interconnect platform for communication in many/multi-core systems. In NoC

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