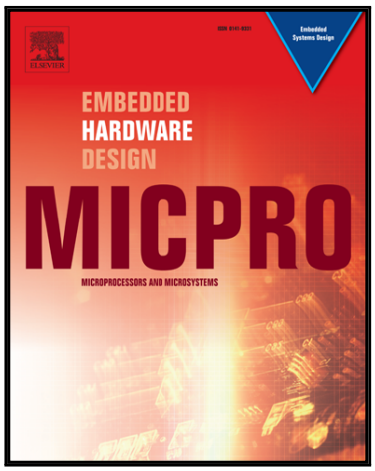

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Improving the Area of Fast Parallel Decimal Multipliers

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Abstract

Financial and commercial applications depend on decimal arithmetic because they must produce results that match exactly those obtained by human calculations. Decimal multiplication is a frequently used operation in these applications and also in the design of decimal floating-point units. In this paper we propose a new architecture for parallel decimal multiplication that improves the area of previous decimal multipliers while keeping the best performances. A decimal adder [1] based on a mixed BCD/excess-6 representation of the operands is utilized. A new partial product generation unit is proposed based on a 5221 recoding of the multiplier digits. With the proposed multiplier, we are able to improve on state-of-the-art parallel decimal multipliers targeting LUT-6 FPGAs. Compared to previous decimal multipliers, implementation results for 2, 4, 8, 16, 32 and 34-digits show that the proposed multiplier achieves over 20% better area without performance degradation.

Keywords: Decimal multiplication, parallel multiplication, excess-6 coding, 5221 coding, FPGA.

1. Introduction

The beginning of 2000s was an important mark for decimal computing. Previously, the few attempts to bring decimal hardware to processors were somehow unsuccessful since the tradeoff between applicability and hardware cost did not justify a dedicated decimal arithmetic unit. Starting in 2000s, this scenario has changed with the new financial and business applications

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