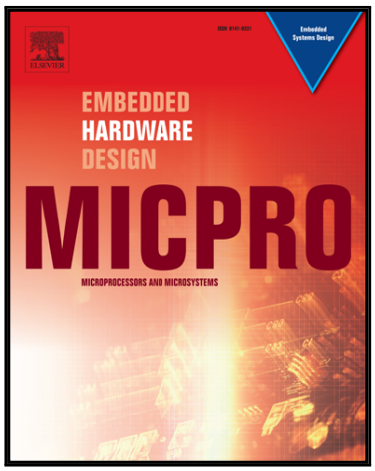

A scheduling based energy-aware core switching technique to avoid thermal threshold values in multi-core processing systems

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ABSTRACT

The increasing on-chip temperature has become a critical issue in the multiprocessor system on chip (MPSoC). It does not only disturb the reliability and performance of the system but it also increases the power consumption. Load balancing is a common scheduling technique to address the thermal issues where the load is transferred to relatively less used cores. However, during the transfer of workload, the destination cores may be in sleep mode and thus take some time to switch to the running mode. It results in wastage of some processing time. This paper presents a thermal-aware load balancing technique that avoids thermal emergencies while eliminating the switching delays. The proposed technique estimates the time taken by a task set to reach the temperature threshold values with the help of offline recorded thermal profiles of datasets. Moreover, cores are selected in a round-robin manner to equilibrate thermal gradients. The technique is based on Global Earliest Deadline First (GEDF) scheduling algorithm and considers ambient temperature, thermal cycles and energy consumption. The proposed technique is tested in a simulation environment comprising of scheduling and thermal simulation model. The results show that the technique reduces the average temperature up to 17%, thermal cycles up to 15%, energy consumption up to 20% and lowers the temporal and spatial gradients as compared to the commonly used predictive thermal-aware and thermal balancing techniques.

1. Introduction

Embedded systems have become an integral part of the modern life from commonly used household appliances and vehicles to the military equipment and spaceships. It is predicted that almost 40 billion embedded devices will be available in the world till 2020 [1]. The ever-increasing complexity of the firmware due to the complex nature of applications requires more sophisticated processing units with higher processing capabilities. Consequently, this scenario has resulted in the introduction of the multi-core system in place of single processing systems.

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Although a large number of cores operating at superior clock speed have significantly improved the performance of the system, but it incurred some undesirable effects in the system. The thermal emergencies, being one of them, have become more critical in this emerging situation. With the noteworthy advancement in fabrication technology, Moore's law [2] is still valid and the size of the transistor is continuously shrinking. It has resulted in an increased value of on-chip power density and reduced surface area for heat dissipation to the external environment. High chip temperature is the overall consequence. Either battery-powered embedded systems or large servers or data centres, the elevated chip temperature brings significant challenges to the system in terms of lower reliability, high power consumption and higher cost.

The reliability of the system is adversely affected by the peak temperature. The mean time to failure (*MTTF*) of the device is described by equation 1.

$$MTTF = a.e^{E_a/K.T} \quad (1)$$

where a is the constant, ??$_a$ is the activation energy in electron volt (eV),