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Real-time HDTV to 4K and 8K-UHD conversions using anti-aliasing based super resolution algorithm on FPGA

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ABSTRACT

The demand for light-weight and high-speed super resolution (SR) techniques are growing because of super high-resolution displays, such as 4K/8K ultra high definition televisions (UHDTVs), which have become common. We propose a single pass over up-sampled anti-aliasing based SR method. Our method can attenuate jaggies and perform natural-looking contrast improvement focusing only on the shadow part in the edge of an enlarged image without the need to preserve the entire enlarged image. Therefore, this method is suitable for hardware implementation, and the proposed architecture requires five-line buffers only (in the memory section). We implemented the proposed method on a field programmable gate array (FPGA) and demonstrated HDTV-to-4K and-8K SR processing in real time (60 frames per second).

1. Introduction

Super high-resolution displays such as retina displays and 4K/8K ultra high definition televisions (UHDTVs) have been spotlighted among digital home appliances [1]. Thus, super resolution (SR) techniques, which increase the resolution of images, are necessary for transcoding existing low-resolution media on high-resolution displays. An SR system has to be implemented on hardware if the appliance requires real time processing, where the system produces outputs simultaneously with the inputs in finite latency. SR techniques that utilize videos have been proposed in the literature [2,4]; however, they require multiple frame buffers and are thus unsuitable for compact hardware implementation. Therefore, in this paper, we focus on single-image SR. Single-image SR can roughly be categorized into three types: i) interpolation-based, ii) reconstruction-based, and iii) statistical or learning-based single-image SR (e.g., see [5,6]). Interpolation-based algorithms utilize digital local filters such as bilinear filters, bi-cubic filters, and Lanczos filters for interpolation of missing pixels, which cause blurring and aliasing in the resulting image. Reconstruction-based algorithms solve the optimization problem to reconstruct edges on images through many iterations of incremental conversions between high-resolution and low-resolution images. Statistical or learning-based algorithms construct high-resolution image libraries through iterative learning. These three approaches may not fully satisfy both the frame-rate and image-quality constraints of today's digital home appliances.

Recently, in the learning-based single-image SR [7,8], deep learning method, which is Super-Resolution Convolutional Neural Network (SRCNN), has been proposed and has attracted attention. SRCNN consists mainly of three processes - patch extraction, nonlinear mapping and reconstruction. When a low-resolution image is input to SRCNN, local features are extracted as the patch library in the first convolutional layer. Then, in the second layer, these features are nonlinearly mapped to the high-resolution patch representation. Finally, in the third layer, the high-resolution image is generated by its surrounding predictions. This method can generate high quality images with high PSNR values. However, this method requires enormous memory resources and calculation cost. For this reason, its implementation has been limited to the software.

We have studied anti-aliasing SRs for obtaining smooth edges [9,10]. In this paper, we present an FPGA-based SR implementation which generates not only jaggy-less edges using anti-aliasing, but also the output images have natural-looking edges. The remainder of this paper is organized as follows. Our super resolution algorithm is described in Section 2, and the FPGA implementation is presented in Section 3. In Section 4 we discuss our experimental results using a performance summary table, and conclude this work in Section 5.

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2. Our super resolution algorithm

2.1. Related work

Surveying the current literature results in many related works. A hardware based SR system is presented in [11] which makes use of existing motion estimations from a decoding block and aims to minimize the memory cost. This proposed system makes use of very long instruction words (VLIW) and ARM processors. No deblurring or image sharpening is performed in this work. In [12] an FPGA- based iterative back projection (IBP) method is presented. This architecture requires memory access to all low-resolution (LR) frames used in the high-resolution (HR) estimate, and results are computed only after multiple passes through the hardware. This implementation reaches operating frequency of 80 MHz. According to authors [12] this is sufficient to allow real-time execution outputting 25 VGA 2× super resolved frames, allowing implementation of a maximal of 10 iterations. The drawback of this implementation, according to authors of [13], are high memory requirements and the fact that, in order to output a super-resolved image, multiple passes through the hardware are required. The work in [13] reports FPGA implementation of a super-resolution image reconstruction based on IBP. In this approach, additional details are reconstructed based on exploitation of sub-pixel shifts caused by warping ([14]). The processing is done at pixel level by means of weighted mean optical flow, denominated weight based picture elements (pels) merging. Weight are estimated based on the inter-frames motion estimations for pel patch matching. The proposed architecture, implements 10 iterative stages, mapped on the FGPA device reaching a frequency of 58 MHz. In their configuration the system was could super-resolve 61 CIF LR images to 1280 × 720 pels per second. However, satisfactory quality level requires 20 iterations, which appears to be beyond the capability of the supporting device. This limitation is due to the on-chip memory constraint. In [15] Szydik et al. proposed a non-iterative approach. However, their results report only QCIF to CIF super resolution for 25 FPS. According to the authors, their implementation is not scalable and limited to work with only two reference frames.

Gohshi et al. proposed a non-iterative algorithm for single- image SR [16]. Their processing flow is illustrated in Fig. 1. After applying an interpolation filter, the algorithm performs edge detection and edge enhancement by high-pass filtering (HPF) and cubic function. This algorithm seems to be suitable for hardware implementation because it does not require iterations (and thus no frame buffers), while exhibiting better performance when compared with the performance of other conventional interpolation-based algorithms, by reproducing the frequency spectrum exceeding the Nyquist frequency. The Lanczos filter will generally be utilized for the interpolation of input images; however, upon implementing the hardware, the filter requires many floating-point operations on wide filter kernels (Lanczos 3: 6 × 6) [17]. Moreover, line buffers are also needed between the interpolation stage and the edge-enhancement stage. In this paper, we propose a novel SR algorithm, which is based on the anti-aliasing method, it performs direct calculation of the anisotropic interpolation, local-statistics-based edge reconstruction and natural-looking edge enhancement, while requiring only five-line buffers. Our contributions are as follows:

i) Anti-aliasing based SR method with redundant internal resolution and post down-sampling, whose output are less jagged.
ii) Low calculation cost edge reconstruction, utilizing local statistics.
iii) Natural-looking edge enhancement based on asymmetric weighted halo components.
iv) FPGA implementation for real-time HDTV to 4K- and 8K UHD conversion and its demonstration.

2.2. Proposed super resolution (SR) algorithm

Fig. 2 shows the concepts of our single-pass SR algorithm, that requires no frame buffers. With SR algorithms, it is difficult to construct good edges. Multi sampling with anti-aliasing makes jaggy free edges and this algorithm uses that concept. However, with jaggies it is easy to perform over enhancement. Additionally, we can apply simple edge enhancement techniques. In this method, an over-sampled image with jaggies is compressed into target resolution for suppressing them. Also, our algorithm generates an over up-sampled image, enhances the edge until the jaggies occur, and compresses the image into the target

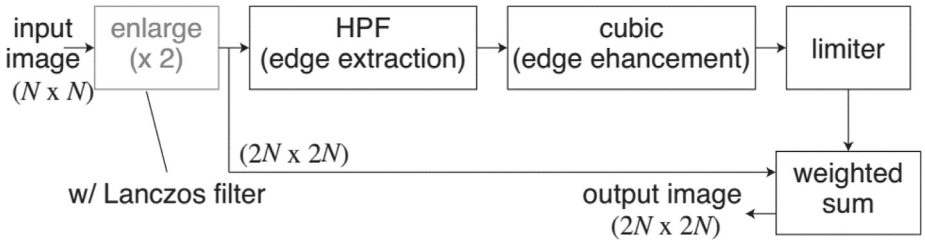

Fig. 1. Goshi's single image super resolution model [1].

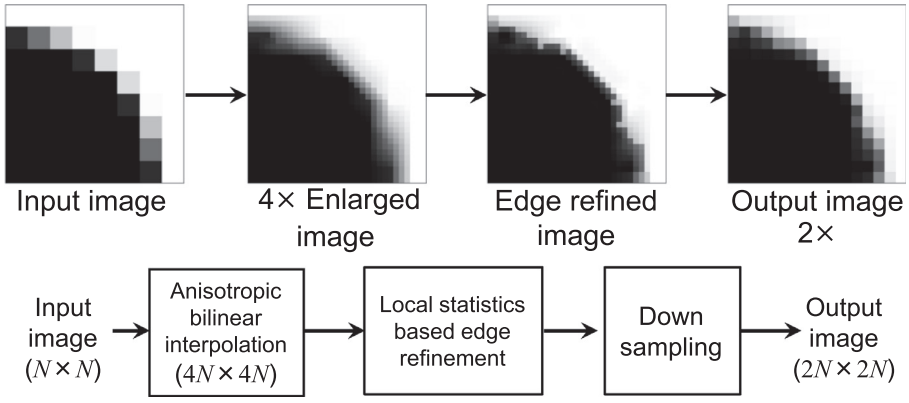

Fig. 2. Processing flow of the proposed anti-aliasing based SR algorithm.