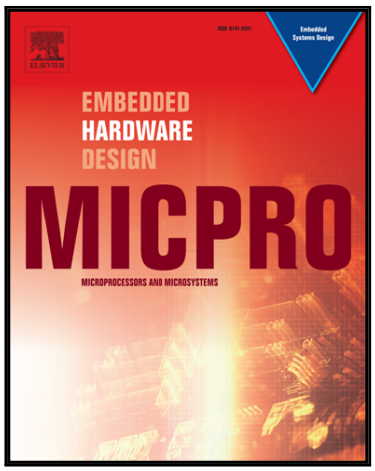

Fast and Efficient Power Estimation Model for FPGA based Designs

Abhishek N. Tripathi , Arvind Rajawat

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Abhishek N. Tripathi, Dept. of ECE, MANIT Bhopal (M.P.), India
abhi.sanutripathi@gmail.com
Arvind Rajawat, Dept. of ECE, MANIT Bhopal (M.P.), India
rajawata@manit.ac.in

Abstract

With the growing scope of embedded computing, specific design objectives demand quick exploration and estimation of design metrics. Power estimation is one such primary design metric which needs to be estimated at the earliest stage of high-level design. In this paper, a model is presented to estimate dynamic power requirement of any given application for a target field-programmable gate array (FPGA) device. The methodology comprises of the profiling of the C/C++ programs through a low-level virtual machine (LLVM) pass and training of an artificial neural network model using the profiling results to estimate power. For profiling an application, the LLVM based framework is employed, which generates target independent LLVM intermediate representation (IR). A module pass is written to obtain the count of the different type of instructions. A model using artificial neural network has been proposed to give the power estimate, which takes as inputs the category-wise number of instructions and FPGA target resources on which the respective applications are mapped. The Zynq family device is profiled using Vivado HLS v.2015.4. The model has been validated against CHStone benchmark programs. Furthermore, a reduced relative error of 0.19% to 7.9% is observed for the analyzed benchmark designs, with the exceptional increase in estimation speed, which is more than the order of magnitude of the conventional Xilinx Vivado Design Suite. Therefore, for designers, this modeling methodology provides better, accurate and fast power estimation, at the early stage of the VLSI design.

Keywords: Design space exploration, High-level synthesis, Power estimation, Field programmable gate array (FPGA), Low level virtual machine intermediate representation (LLVM IR), Artificial neural network (ANN).

1. Introduction

The current trend of Internet-of-Things (IoT), results in the extensive usage of fast computing embedded devices in all fields [3], [9]. FPGA-based design is a preferable choice for faster time to market. Design metrics for these FPGA designs need to be explored in early stages of the VLSI design. Power estimation is one of the major design metrics for the designers. At the system- level, although the power can be determined quickly, but at the cost of accuracy. System-level enables the evaluation of design quality in terms of estimated power, thereby enabling the exploration of design decision prior to the final implementation. Currently, high-level synthesis is used to transform the application into the final implementation [4], [12], [15], which creates a need for early power estimation. Modeling of hardware (HW) and