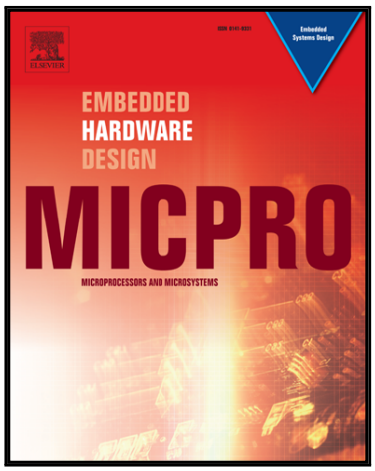

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Abacus turn model-based NoC routing for interconnects with switch or link failures

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Abstract

With the aggressive scaling of the VLSI technology, Networks-on-Chip (NoCs) are becoming more susceptible to faults. Therefore, designing reliable and efficient routing methods is of significant importance. Most of the existing fault-tolerant techniques rely on rerouting solutions which may degrade the network performance drastically not only by taking unnecessary longer paths, but also by creating hotspots around the faults. Moreover, such off-line techniques cannot adapt to the dynamic traffic distribution in the network. In this paper, a reconfigurable and deadlock-free routing method is proposed based on the Abacus Turn Model (AbTM) to tolerate single and double switch or link failures. The required resources are kept to a minimum by avoiding to use virtual channels and routing tables. The proposed method is able to dynamically adjust the availability of the healthy paths according to the location of failures and congestion in the network to minimize rerouting. Moreover, it can grant a high degree of adaptiveness to the packets. This efficiency makes the proposed method a powerful asset for reliable routing in NoCs. The experimental results demonstrate that an 8×8 mesh network remains 100% reliable against single faults, and 99.8% and 99.94% reliable against double switch and link failures, respectively.

Keywords: Network-on-Chip (NoC), fault-tolerant routing methods,

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