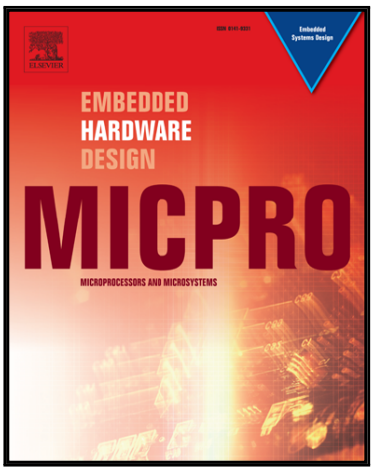


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# A Scalable and Adaptable Hardware NoC-Based Self Organizing Map

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**Abstract**

Due to their ability to reduce the size of high-dimensional input data, Self-organizing maps (SOMs) can be employed as data quantizers. The widely used software implementations of SOM enjoy flexibility and adaptability, usually to the detriment of performances, which limits their use in real time applications. On the contrary, the hardware counterparts of SOMs exploit the inherent parallelism of hardware to boost the overall performances, but generally lack adaptability without considerable design efforts. To benefit from both, the flexibility of software and performances of hardware SOM implementations, unconventional design approaches of SOMs should be used. In this work, a scalable and adaptable hardware implementation of a SOM network is presented. The proposed architecture allows to dynamically extend the SOM operation from a smaller to a larger map only by (re-)configuring the parameters of each neuron. The gained scalability is obtained by decoupling the computation layer composed of neurons, from the communication one, used to provide data exchange mechanisms between neurons. The proposed SOM architecture is also validated through simulation on variable-sized SOM networks applied to image

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