Microprocessors and Microsystems 56 (2018) 92–100

Contents lists available at ScienceDirect

Microprocessors and Microsystems

journal homepage: www.elsevier.com/locate/micpro

Ultra-low voltage and energy efficient adders in 28 nm FDSOI exploring poly-biasing for device sizing

Ali Asghar Vatanjou*, Even Låte, Trond Ytterdal, Snorre Aunet

Department of Electronic Systems, Faculty of Information Technology and Electrical Engineering, Norwegian University of Science and Technology (NTNU), O.S. Bragstads plass 2a, Trondheim, 7491, Norway

ARTICLE INFO

Keywords:
Subthreshold
28 nm FD-SOI
CMOS
Full-adder
Ultra-low power

ABSTRACT

Balancing the PMOS/NMOS strength ratio is a key issue to maximize the noise margin, and hence, the functional yield of CMOS logic gates and minimize the leakage energy per cycle in the subthreshold region. In this work, the PMOS/NMOS strength ratio was balanced using a poly-biasing technique in conjunction with back-gate biasing provided in a 28 nm fully depleted silicon on insulator (FDSOI) CMOS technology. A 32-bit adder based on minority-3 (min-3) gates and a 16-bit adder based on Boolean gates have been implemented. Chip measurement results of nine samples show highly energy efficient adders. The 32-bit and 16-bit adders achieved mean minimum energy points (MEP) of 20.8 fJ at 300 mV and 12.34 fJ at 250 mV, respectively. In comparison to adders reported in other works in the same technology, the energy per 1-bit addition of the 32-bit adder is improved by 37%. This improvement in energy consumption is 25% for the 16-bit adder. According to the measurement results of ten chips, the designed adders exhibited functionality down to supply voltages of 110 mV-125 mV, without body biasing. Additionally, the minimum V_{dd} of all the 32-bit adders based on minority-3 gates decreased to 80 mV by applying a reverse back bias voltage to the PMOS devices. One sample was functional at 79 mV with a 430 mV reverse back bias voltage applied to its PMOS devices.

1. Introduction

Reducing power consumption to ultimately break heat walls or to reduce energy consumption to prolong battery lifetime are key issues in present day microelectronics. The growing number of battery driven wireless devices, as well as the increasing energy demand of the applications to which these are intended, create a need for innovations in ultra-low power (ULP) circuitry. Subthreshold operation, potentially providing higher energy efficiency than other known low power circuits, has been known since the 1960s [1]. However the increasing demand mentioned above, and new features of modern process technologies, brings relevance of subthreshold design back.

A commercially available 28 nm FDSOI CMOS process tackles some of the key challenges faced by the scaling of conventional bulk silicon devices better, and so enables prolongation of Moore's law [2]. In this technology, the junction capacitance is significantly reduced and the drain induced barrier lowering (DIBL) effect is also lowered due to the ultra thin body and buried oxide [2], this while increasing the efficiency of back-gate biasing. In addition, the random dopant fluctuation is suppressed because threshold voltage adjustments do not depend on doping levels.

This manuscript present several extensions to the contents in [3] with respect to both statistical simulations and new measurements on additional chip samples. The extensions to simulations include variability in on-currents and delay as functions of sizing, and how sizing can affect energy per cycle for the designed logic cells. Post-layout simulations were also added, and compared to measurements results. Additionally, new measurements results have been added, which include effects of applying back-gate biasing voltages. Further extensions to [3] include measurements of static power consumption for nine 16-bit and 32-bit adder samples.

We here report highly energy efficient logic gates by exploiting both poly-biasing [4] as well as back-gate biasing techniques. Both techniques allow us to reduce the size of the pull up devices, thus reducing the leakage current and parasitic capacitance of the cells. This in turn leads to reduced power consumption. The poly-biasing technique increases the effective channel gate length without increasing the active area of the devices. Applying poly-biasing while connecting the PWELL/NWELL ties to ground improves the strength of the PMOS transistors. Moreover, the regular threshold voltage (RVT) devices have been chosen to reduce the leakage current further, compared to low threshold voltage (LVT) devices. Although higher threshold voltage

* Corresponding author.
E-mail addresses: ali.vatanjou@ntnu.no (A.A. Vatanjou), even.laate@iet.ntnu.no (E. Låte), trond.ytterdal@ntnu.no (T. Ytterdal), snorre.aunet@ntnu.no (S. Aunet).

https://doi.org/10.1016/j.micpro.2017.11.002
Received 20 February 2017; Received in revised form 2 November 2017; Accepted 8 November 2017
Available online 09 November 2017
0141-9331/

leads to slower circuits, it can reduce the energy consumption of circuits with more relaxed throughput requirements [5]. The computational demands of wireless sensor networks (WSNs) have been discussed in [6], and the sensor-network applications were categorized into three groups: 1- low-bandwidth rates (sample rate less than 100 Hz), 2- mid-bandwidth rates (sample rate 100 Hz-1 KHz) and 3- high-bandwidth rates (sample rate higher than 1 KHz). It was shown in [6] that the performance of a processor with 168 KHz clock was more than four times of the desired performance for mid-bandwidth applications. For such systems with relaxed throughput requirements, a lower static power and robust functionality at ultra-low voltages translates into a lower energy consumption. Moreover, the use of RVT devices enables applying extreme reverse back-bias schemes to save leakage energy in the sleep mode, and avoid costly power-gating.

To validate the proposed sizing techniques, we have implemented a 32-bit adder based on min-3 gates [7] and a 16-bit adder based on traditional Boolean gates. The ripple carry adder (RCA) topology has been chosen because the energy consumption of the serial adders may be lower than the parallel adders while maintaining the same speed, when operated in subthreshold [8]. Comparing to adders reported in the same 28 nm FDSOI process technology [9], the minimum energy per 1-bit addition of the 32-bit and 16-bit adders have been improved by 37% and 25%, respectively.

To the knowledge of the authors, the 32-bit adder provides the lowest energy per 1-bit addition and the lowest functional V_{dd} among static CMOS circuits with more complex functionalities than simple inverters or ring-oscillators.

The remainder of the paper is organized as follows: The device sizing is discussed in Section 2. Two implementations of subthreshold adders are presented in Section 3. Measurement results are shown in Section 4, and is followed by a discussion in Section 5, before the final conclusions in Section 6.

2. Device sizing for balanced PMOS/NMOS

2.1. Transistor dimensions

Balancing the driving strength of the pull-up/pull-down networks (PUN/PDN) is a key issue to properly operate logic gates in the ultra-low voltage (ULV) domain. In addition, unbalanced PMOS/NMOS increases the leakage energy of subthreshold circuits [10]. Nevertheless as shown in Fig. 1, the on-current ratio of the PMOS with respect to NMOS is too small in the ULV domain. In Fig. 1, the NMOS device width is 200 nm, L = 30 nm and the drain-source voltage is set equal to the supply voltage. For example, the PMOS gate width should be upsized by more than 4X to have a balanced PUN/PDN at a supply voltage of 150 mV. This causes asymmetry in the layout of the cells. Additionally, both leakage current and parasitic capacitances, and consequently the power consumption of the circuit, increase with wider PMOS

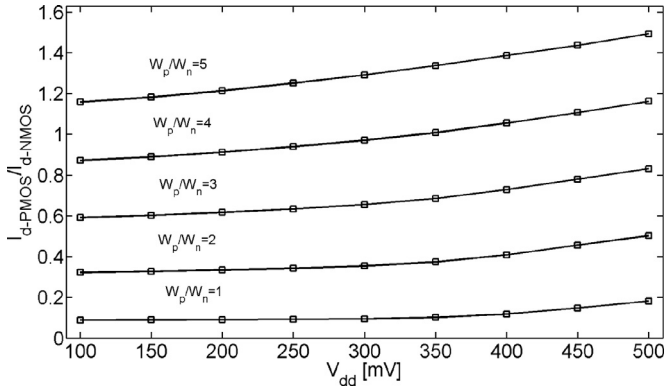

Fig. 1. PMOS/NMOS on-current ratio versus V_{dd} for $W_n = 200$ nm and $L_n = L_p = 30$ nm.

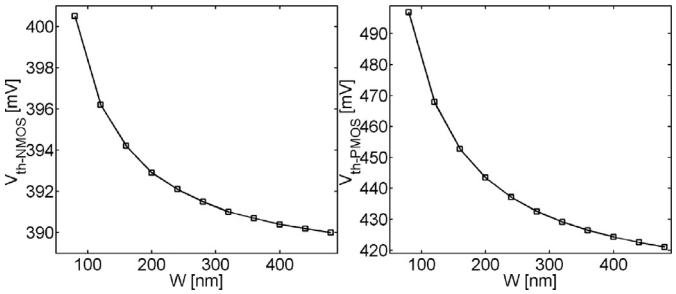

Fig. 2. Dependency of the threshold voltage on channel width (a) NMOS (b) PMOS.

transistors. Therefore using techniques to improve the strength ratio between PMOS and NMOS, can be an effective approach to reduce both power consumption and minimum operating supply voltage of sub-threshold circuits.

In this work we increased the effective gate length of the NMOS transistors by 16 nm using poly-biasing to balance NMOS and PMOS driving strengths. We also connected both NWELL and PWELL ties to ground, thus the bulk-source junction of PMOS transistors were forward biased. In order to reduce the leakage current further, the effective PMOS gate length was also increased by 4 nm using poly-biasing, while maintaining the switching voltage at $V_{dd}/2$. As can be observed from Fig. 2, the threshold voltage of this 28 nm FDSOI technology is inversely proportional to the gate width of the devices. In Fig. 2, $L_{nmos} = L_{min} + 16$ nm, $L_{pmos} = L_{min} + 4$ nm and $V_{dd} = 200$ mV. The NMOS and PMOS transistor channel widths were chosen taking into account the channel width dependency of the threshold voltage. The minimum width of the NMOS devices was chosen to be 200 nm and the corresponding PMOS width that resulted in a switching voltage of $V_{dd}/2$ for an inverter was 300 nm. Although a W_p/W_n ratio of 1.5 is required for balancing the PMOS and NMOS transistors, this is a reasonable ratio comparing with for example [11], where for $W_p/W_n = 5$, PMOS/NMOS strength ratio is balanced and for $W_p/W_n = 2$, the PMOS and NMOS transistors are still unbalanced. Fig. 3 shows the schematics and device sizes for the basic logic cells that were used to implement the 1-bit full adders (FA).

2.2. Exploring variability and energy efficiency

In order to explore the robustness of the proposed sizing approach, the drain current variability of an inverter (INV3) based on the proposed sizing approach was simulated and compared to two other inverters. The drive strength of the pull-up/down devices of the first inverter (INV1) were balanced and the active area of the PMOS was more than 5X the NMOS active area with $W_P = 420$ nm, $W_n = 80$ nm and $L_P = L_n = 30$ nm. The second inverter (INV2) had the same total area as INV1 but the PMOS/NMOS drive strengths are not balanced ($W_P = 300$ nm, $W_n = 200$ nm and $L_P = L_n = 30$ nm). The active area of the PMOS in INV3 is only 1.1X the NMOS active area where $W_P = 300$ nm, $W_n = 200$ nm, $L_P = 30 + 4$ nm and $L_n = 30 + 16$ nm.

Fig. 4 shows the NMOS/PMOS on-currents variability for the above discussed inverters as a function of supply voltage. Monte Carlo

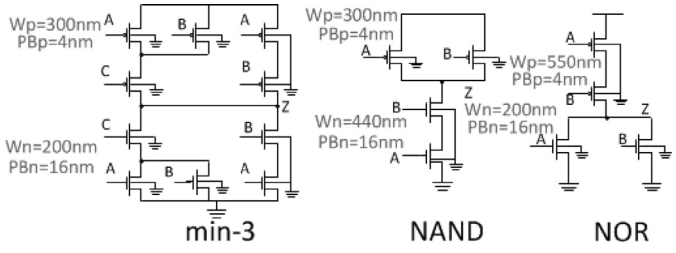

Fig. 3. Schematic view and corresponding device sizes of the basic logic gates used to implement FAs.