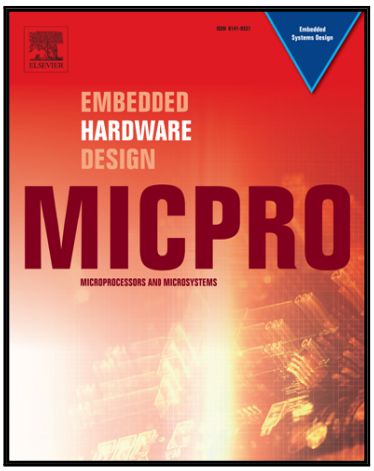

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Decimal Addition on FPGA based on a Mixed BCD/Excess-6 Representation

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Abstract

Decimal arithmetic has recovered the attention in the field of computer arithmetic due to decimal precision requirements of application domains like financial, commercial and internet. In this paper, we propose a new decimal adder on FPGA based on a mixed BCD/excess-6 representation that improves the state-of-the-art decimal adders targeting high-end FPGAs. Using the proposed decimal adder, a multioperand adder and a mixed binary/decimal adder are also proposed. The results show that the new decimal adder is very efficient improving the area and delay of previous state of the art decimal adders, multioperand decimal addition and binary/decimal addition.

Keywords: Decimal addition, parallel addition, binary/decimal addition, multioperand addition, excess-6 coding, FPGA.

1. Introduction

Computer arithmetic is predominantly based on binary arithmetic since its numerical properties are easier to implement in hardware when represented in radix-2 than in radix-10. However, decimal arithmetic is a requirement in the computation of many applications, like financial and commercial, where the results must match those obtained by human calculations. In many databases of these applications, numbers are in decimal format. Since many decimal numbers cannot be represented exactly as binary numbers with a finite number of bits, arithmetic operations must be done directly over decimal

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