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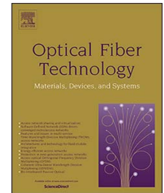

Invited Papers

Silicon photonic terabit/s network-on-chip for datacenter interconnection

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ABSTRACT

Silicon photonic integration is an enabling technology for power- and cost-effective optical interconnects in exascale performance computers and datacenters which require extremely low power consumption and dense integration for a higher interface bandwidth density. In this paper, we experimentally demonstrate a fully integrated optical transceiver network on a silicon substrate using heterogeneous integration. High performance on-chip lasers, modulators and photodetectors are enabled by transferring III–V materials to a pre-patterned silicon substrate. Wavelength division multiplexed transceivers with eight wavelength channels are monolithically-integrated on a single chip, forming an optical network-on-chip circuit with total transmission capacity up to $8 \times 8 \times 40$ Gbps, and bandwidth density over 2 Tbps/cm. We show that the heterogeneous silicon integration provides the design flexibility and scalability for high-speed optical communication systems.

1. Introduction

The demand for fast, reliable, and low-cost optical data links has led to research in developing the next generation of photonic integrated circuits (PICs) to improve the power efficiency, latency, and capacity. In past decade, the power required for photonic transmission in data centers and supercomputers has been dramatically reduced in energy per bit. The transmitter size per capacity has been reduced by a factor of 10–100, and in the same time the bandwidth capacity has been increased from 10 Gb/s to 400 Gb/s in short links. However, the typical energy consumption of 10–100 pJ/bit to date must shrink further by another 2 to 3 orders of magnitude within the next few years for practical optical interconnection applications [1,2]. This demand can be achieved with complete integration with a high bandwidth density, low power module, and most importantly a low-cost package technique.

Silicon photonics has shown its great potential for monolithic integration with the well-developed complementary metal–oxide–semiconductor (CMOS) fabrication [3–7]. Benefiting from the low loss of Si and advanced process techniques, a variety of functional components, including low loss waveguides (WGs) [8,9], modulators [10–12] and photodetectors [13–15] have been developed on the silicon-on-insulator (SOI) platform. Monolithic integration of photonic components with the electrical driver and/or other logic circuits were demonstrated on silicon with a standard semiconductor foundry process [16–18]. As an example, Ref. [18] presented the first single-chip microprocessor with embedded optical interconnection between processor core and memory bank with on-chip modulators, photodetectors and off-chip light source. Such approach requires co-design and co-process of optical and electrical components, and in many cases compromises must be made between the two parts of the system. Therefore, it is better to optimize and fabricate the photonic chips and driver circuits individually, and then integrate both circuits together with 2.5D or 3D architecture in a compact chip package [19,20]. Advanced signal multiplexing techniques are normally involved in the photonic circuit design to scale up the chip bandwidth. In particular, integrated wavelength division multiplexing (WDM) systems combined with single mode fiber shows great advantages compared with discrete links such as vertical cavity surface emitting laser (VCSEL) links in short distance communication [21–23].

However, the lack of a reliable silicon laser has been the major impediment due to the fundamental material limit of silicon, which has an indirect band-gap. Three approaches have been widely used to achieve an on-chip laser by introducing efficient light emission materials on silicon with three major approaches: (1) hybrid, (2) heteroepitaxy or (3) heterogeneous integration. The hybrid assembly approach couples the laser output from a III–V chip with gain section into the silicon chip laterally [24,25] or vertically [20,26]. This approach allows optimization and fabrication of the III–V and silicon chips individually, but it is mainly limited by the complications in light coupling and device packaging, as well as the extra fabrication cost of two separate chip fabrication. Direct epitaxial growth of III–V materials, especially quantum-dot (QDs) gain materials on silicon is a promising solution for high performance lasers with high volume throughput

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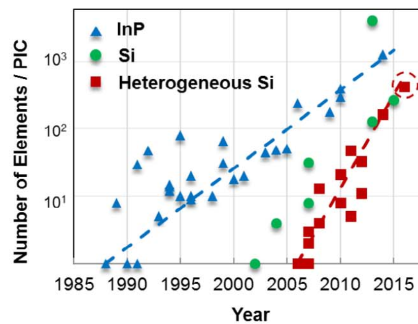

Fig. 1. Evolution of photonic integration in terms of the number of devices on a single waveguide on chip. Silicon photonic (green circle) represents the "passive" integration without an on-chip laser; InP integration (blue triangle) and heterogeneous silicon integration (red square) have integrated active devices including lasers on-chip. The circled data point indicates the PIC reported in this work. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

[27–31]. However, the lifetime and reliability of the heteroepitaxial lasers require further improvement. Moreover, heteroepitaxial growth normally has a thick or dedicated buffer layer to annihilate the propagating dislocations from the heterogeneous interface, which makes it difficult to couple the laser output into the waveguide at the silicon layer. In this paper, we focus on the heterogeneous silicon integration (HSI) approach, which transfers the functional materials to silicon with a wafer bonding technique [32–37]. By using a selective die bonding method, which selectively places a number of small III–V chips to designated zones on a large silicon wafer, the total cost can be dramatically reduced, and multiple functionalities can be realized by integrating different epitaxial structures on the single chip [38]. This platform is not limited to the integration of III–V materials, but can be applied to a wide variety of material systems to integrate nonlinear and nonreciprocal materials for many different applications [39–42].

Fig. 1 shows the evolution of InP- and silicon- based photonic integration platform in terms of the number of devices integrated on one chip, representing "Moore's Law" in the photonic integration field. With more and more photonic devices integrated on the single chip, both the complexity and functionalities of the PICs have been greatly improved in past three decades. Silicon photonic integration is catching up with InP-based III–V photonic integration. Benefitting from the compact component footprint and low loss waveguide, over 4000 devices were integrated in the large-scale silicon phase tuning array chip in 2013 [43]. Particularly, with an efficient on-chip laser solution, the HSI platform has been rapidly growing since its invention in 2006. This paper will summarize the design and demonstration of our recent advances on heterogeneous integrated optical network-on-chip (ONoC) circuit [44]. With eight transceiver nodes and over 400 photonic components in a single die, large communication capacity was achieved for the application of high-speed datacom interconnects in high performance computers (HPCs) and data centers. The remainder of this paper is organized as follows: Section 2 shows the architecture of the ring optical network. Section 3 discusses the photonic circuit design and fabrication process. Section 4 and 5 report the characterization of key components and the optical network circuit, respectively. Finally, Section 6 summarizes this paper.

2. ONoC architecture

The ONoC topology defines the structure of the network and controls how data flows among the transceiver nodes in the network. A number of ONoC topologies have been reported [45–49], such as Corona [45], Firefly [46], ATAC [47], etc., typically designed for a multi-core system with 2-D or 3-D photonic integration. In the case of the Corona network, the WDM clusters are connected to bus waveguide with resonator structures [45]. As a wavelength-selective switch (WSS) component, the microring resonator picks up one channel of the WDM spectrum as either modulator/multiplexer (Mux) or photodetector/demultiplexer (DeMux). However, the bandwidth at each node is limited by the modulation speed and the optical bandwidth of the microrings.

In this paper, to overcome this bandwidth limit, we propose a ring network architecture based on broadband optical switches instead of WSS components. The network architecture has a ring topology with circular and close bus waveguide as the basic infrastructure, as schematically shown in Fig. 2. Multi-nodes of photonic WDM transceivers are attached to the bus through broadband optical routers/switches. The transmitter/receiver nodes have individual electrical/optical (E/O) interface to CMOS driver and the corresponding clusters. Two spare nodes in this chip are present as optical interface for coupling with single mode fibers. The broadband optical routers/switches control all the WDM channels simultaneously to scale up the total bandwidth at each node.

Such ring architecture defines a reconfigurable network that can be controlled by varying the working status of the optical routers, as illustrated in Fig. 3. With a normally-off switch design, the default mode is at self-communication or self-configuration status, where the transmitter is talking to its local receiver for self-testing or initialization (Fig. 3(a)). By fully turning on any two of the switches in the network, all WDM channels at one transmitter or from the off-chip optical interface can be routed to another node simultaneously, as a cluster-to-cluster or point-to-point mode (Fig. 3(b)). It can also work in a

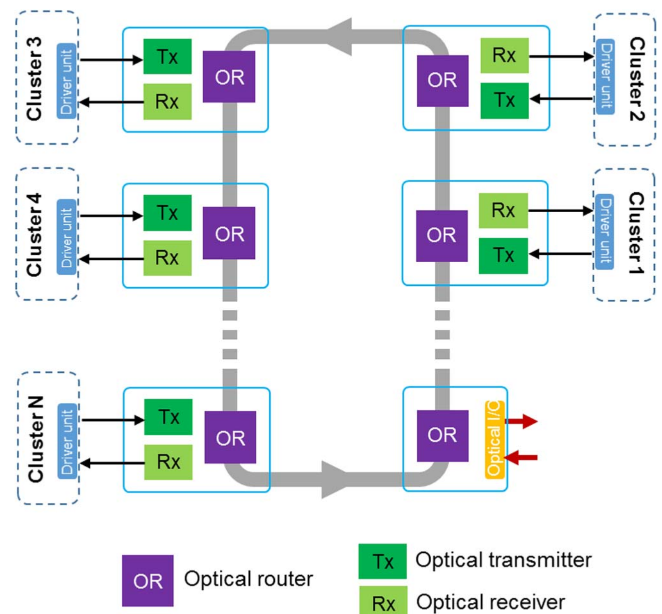

Fig. 2. Architecture overview of the ONoC circuit.

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