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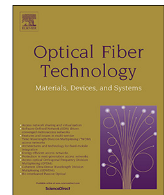

Regular Articles

Invited Paper: Automated, high-throughput photonic packaging

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A B S T R A C T

Silicon photonics can enable optical circuits of unprecedented complexity and cost efficiency. It employs lithography to effectively pre-assemble optical devices on wafers fabricated in existing microelectronic facilities with decades of cost and reliability optimization. Unfortunately, the packaging of photonic chips still employs legacy approaches, which limit the device's cost efficiency and scalability. To address this challenge, we have developed a novel approach to photonic packaging centered on shifting complexity from chip-level assembly to wafer-level planar fabrication. Self-alignment structures and large-mode converters are integrated on chip to enable photonic packaging in standard, automated, high-throughput microelectronic assembly tools. We demonstrate solutions to interfacing standard optical fibers to chips and to interfacing photonic chips to other photonic chips. We show wide spectral bandwidth and a peak transmission of −1.3 dB from a standard fiber patch cable to chip and −1.1 dB from chip to chip. We believe this new direction can help silicon photonics reach its full potential.

1. Introduction

Cost is more than a commercial consideration. It can define the accessibility of a technology and, in turn, it's societal impact. This notion is well illustrated with green technologies. Achieving attractive performance is one challenge. However, even with great performance, a technology's green impact will not be sizeable without a cost point enabling widespread adoption.

The same reasoning can be applied to optical fiber technology. With communication bandwidths per fiber surpassing tens of terabits [1], performance does not appear to be what is restraining further societal impact. Rather, we need to consider the cost of the underlying optical devices as limiting their accessibility and preventing widespread use beyond key applications such as the communication backbone. To broaden the societal impact of complex optical devices, they need to be made accessible to a wider spread of applications, which requires a disruptive reduction in cost.

Silicon photonics has the potential to deliver such disruptive cost reduction to complex optical circuits. Legacy devices are made of discrete components that are often individually packaged, manually assembled, and manually tested. This process is expensive and not easily scalable. Photonic integration employs lithography to pre-assemble optical devices on a chip. This reduces the number of components and the corresponding cost of their individual packaging, assembly and testing. Silicon photonics adds to photonic integration by providing chip fabrication that is reliable and economical [2–4]. This allows large complexity at small cost.

The potentially disruptive character of silicon photonics lays in two principles:

1. Shift complexity from assembly technology to planar fabrication technology. Wafer-scale processes are inherently more cost efficient and scalable than chip-scale or device-level processes. Hence, shifting complexity to planar fabrication generally results in

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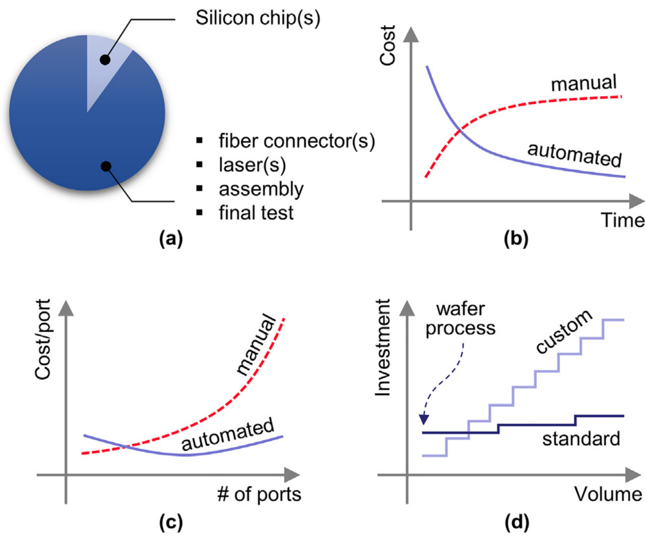

Fig. 1. Schematic illustrations of trends in photonic packaging. (a) Cost structure of silicon photonic devices. (b) Cost of manual labor and automation with time. (c) Cost scaling of automated assembly and manual assembly with device complexity. The lower yield of manual assembly puts it at a disadvantage for complex devices. (d) Scaling with production volume of the required investment for automated assembly with custom photonic assembly tools and existing, standard microelectronic assembly tools.

improved cost and scalability at high volume.

2. Leverage existing microelectronics fabrication facilities to build upon decades of cost and yield optimization. CMOS fabrication technology is far ahead of competing planar fabrication technologies when yield, complexity, and cost per area are considered.

Nonetheless, there is more to a silicon photonic device than the silicon chip, and legacy cost elements are currently limiting the scalability and cost efficiency of silicon photonics. The schematic cost structure of a silicon photonic device is shown in Fig. 1(a). As long as we define silicon photonics as photonics fabricated in a CMOS foundry, and not simply photonics on a silicon wafer, we find that the cost of the complex silicon chips is small when compared to their optical packaging, which still relies on legacy components and legacy processes such as active alignment and manual assembly.

We could ask ourselves if it would be possible to extend the principles responsible for the disruptive character of silicon photonic chips, as presented above, to their packaging. Such approach would entail:

1. Shifting complexity from assembly to planar fabrication technology. Wafer structures would dictate alignment accuracy to avoid expensive high-accuracy placement processes.
2. Leveraging existing high-throughput, automated microelectronics assembly facilities for photonic packaging.

High-throughput microelectronic assembly tools are not a natural choice for photonic packaging due to their limited placement accuracy and inflexible pick-and-place handling. A typical high-throughput tool will provide ± 10 µm placement accuracy while ± 1–2 µm or better is required for single-mode assemblies. To bridge this gap, we integrate self-alignment structures on wafer to dictate alignment accuracy and, by the same token, shift complexity from assembly to wafer technology. In addition, high-throughput tools rely exclusively on vacuum pick-tip handling, which is not well suited to manipulate fibers. These tools also show a pressure sensing movement in the vertical direction only, while fine displacements in more than one axis are required for fiber positioning. These handling challenges are addressed with customized pick-tips and substrate holders that are installed at low-cost in high-throughput tools to enable them for photonic assembly.

The trends among various approaches to photonic packaging are illustrated in Fig. 1(b)–(d). With time, the cost of labor has been historically increasing and is further expected to tick upwards as labor rates in emerging markets catch up with industrialized economies [5]. In contrast, the cost of automation has been decreasing with the cost of underlying electronics. In addition, automation provides better and more consistent yield than manual assembly resulting in better scalability in achievable device complexity. In sum, despite manual assembly still remaining surprisingly affordable, automation is set to take over with time and increasing device complexity. In fact, even legacy manual assembly processes are seeing partial automation today with an increasing number of key process steps being automated for yield or efficiency.

The tradeoffs between approaches to full automation are shown in Fig. 1(d). The use of custom automated equipment requires constant capital investment in additional tools for increased production. This is not the case for standard automated equipment. In fact, even large photonic volumes are relatively small in microelectronic terms and could initially fit in the unfilled capacity of most microelectronics assembly lines without the purchase of additional equipment. This reduces volume-driven investment to enabling jigs and partial tool amortization. With increasing volume, the wafer-level investment required by standard tools is amortized and the use of standard automated equipment shows a growing advantage.

These tradeoffs are summarized in Table 1. The advantage of manual assembly is low initial investment in both capital equipment and chip-level structures. The down side is limited scaling in complexity, due to its lower yield, and slow scaling in volume, which is limited by the availability of skilled labor. For automated assembly in custom tools [6], the scalability in complexity is improved by higher automation yield but the scaling in volume is limited by the capital-investment required. For automated assembly in standard microelectronic tools, the capital investment is small, as the photonic volumes can be accommodated within the volume margins of existing microelectronic facilities, but a wafer-level investment is needed. This investment, however, is insensitive to device volume and the number of ports per device resulting in excellent scalability in both volume and complexity.

A comprehensive solution to photonic packaging must include two parts:

1. Cost-efficient optical inputs and outputs interfacing optical fibers to photonic chips.
2. Cost-efficient integration of multiple photonic chips that are optically and electrically interconnected.

The required number of optical fiber ports and the needed spectral bandwidth per port can be inferred from high-volume core and emerging applications. These are summarized in Table 2 based on Refs.

Table 1
Tradeoffs among various approaches to photonic packaging.

	Capital investment	Wafer-level investment	Scaling in complexity	Scaling in volume
Manual assembly	$	$	Yield-limited	Slow, limited
Automated assembly, custom tools	$$$	$$	Good	Capital-limited
Automated assembly, standard tools	$	$$$	Good	Excellent

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