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Regular Articles

An optimized routing algorithm for the automated assembly of standard multimode ribbon fibers in a full-mesh optical backplane

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ABSTRACT

In this paper a parametric, modular and scalable algorithm allowing a fully automated assembly of a backplane fiber-optic interconnection circuit is presented. This approach guarantees the optimization of the optical fiber routing inside the backplane with respect to specific criteria (i.e. bending power losses), addressing both transmission performance and overall costs issues. Graph theory has been exploited to simplify the complexity of the NxN full-mesh backplane interconnection topology, firstly, into N independent sub-circuits and then, recursively, into a limited number of loops easier to be generated. Afterwards, the proposed algorithm selects a set of geometrical and architectural parameters whose optimization allows to identify the optimal fiber optic routing for each sub-circuit of the backplane. The topological and numerical information provided by the algorithm are then exploited to control a robot which performs the automated assembly of the backplane sub-circuits. The proposed routing algorithm can be extended to any array architecture and number of connections thanks to its modularity and scalability. Finally, the algorithm has been exploited for the automated assembly of an 8x8 optical backplane realized with standard multimode (MM) 12-fiber ribbons.

1. Introduction

In high bandwidth ICT apparata (e.g. data centers, servers, routers) and high performance computing systems, high capacity optical interconnections have now become mandatory [1]. Electrical solutions based on printed-circuit-board (PCB) have now reached their limits in terms of power dissipation and transmission capacity [2,3]. Optical systems provide a valuable alternative thanks to their higher transmission bandwidth, immunity to electromagnetic interferences, and reduced thermal loads and power dissipation due to the exploitation of vertical cavity surface emitting lasers (VCSELs) [3–7]. Yet, in developing new and effective optical interconnection systems, critical issues such as industrial technological feasibility and related production costs should be carefully evaluated [8,9].

Referring specifically to optical backplanes, which interconnect many optoelectronic cards, several solutions have been recently proposed. Besides optical waveguides embedded in standard FR4 boards [8–10], which yet suffer from relatively high attenuation, external optical circuits, both flexible and frame-based, have been presented. In flexible circuits, optical fibers are routed and bonded on a flexible substrate (i.e. polyamide sheets), polished and then terminated with standard connectors [11–14] while in frame-based circuits optical fibers are encapsulated inside a stiffer housing and connected to the backplane with mechanical and optical interfaces [15,16]. However, the abovementioned solutions do not provide a full-mesh connection architecture and mechanically reliable interconnections. Moreover, they do not allow an easy and cheap maintenance because when a failure occurs the entire optical circuit has to be replaced with time-consuming operations which entail the out-of-service of the entire ICT apparatus. In [17] authors have proposed a new optical backplane solution relying on standard multimode (MM) fiber ribbons and multi-fiber push on (MPO) connectors, which solves prior art drawbacks mentioned above [18].

In this paper the authors describe the routing algorithm developed to perform the automated assembly of the proposed backplane, suitable to high-volume manufacturing and optimized to ensure good overall transmission performance. In Section 2 the mathematical formulation of the routing is presented, while in Section 3 the proposed routing algorithm and the related automated assembly method are described. In Section 4 the algorithm optimization is detailed. Section 5 highlights the modularity and scalability of the proposed approach. Finally, Section 6 describes the realization of an optical backplane prototype for

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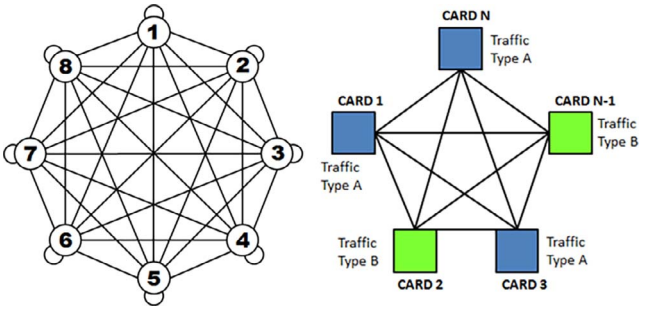

Fig. 1. Full-mesh architecture.

high capacity ICT apparata.

2. Mathematical formulation

2.1. Backplane optical interconnection topology

Fig. 1 schematizes the optical backplane proposed in [17], characterized by a full mesh topology, where each card is connected to other cards through MM fiber optic ribbons terminated with standard MT (mechanical transfer) ferrule [19] and MPO connectors [20]. Each card (node) can transmit data to any other card with bidirectional connections.

With respect to a "Dual-Star" configuration the "Full-Mesh" architecture does not require a centralized switching unit, with a significant cost reduction when the system is not fully employed. In the "full-mesh" architecture each card has its own switching capability and the apparatus can be initially configured with a minimum number of interfaces which can be subsequently increased following customer requirements (Pay as you grow). In addition, the full-mesh architecture makes the system fully transparent with regards to signal bit rates and formats.

2.2. Representation by graph theory

The entire optical interconnection circuit can be mathematically defined as a digraph:

$$G = (C,L)$$

where C is the set of cards of the system (graph nodes) and L is the set of optical links between cards (graph edges). The graph that represents the backplane optical circuit with N cards can be defined as follows:

$$C = \{c_1,c_2,c_3,c_4,c_5,c_6,\ldots,c_{N-1},c_N\}$$

$$L = \{(c_1,c_1),\ldots,(c_1,c_N),\ldots,(c_{N-1},c_N),(c_N,c_N)\}$$

where C is the set of N cards and L is the set of N^2 optical connections between cards. The order of the graph is the number of cards and it can be indicated as follows:

$$N = order(G) = |C|$$

while the graph size is defined as:

$$M = size(G) = |L| = N^2$$

In a full-mesh architecture, each card is connected to all other cards by a straight connection and this can be written as follows:

$$(c_i,c_j) \in L \qquad \forall\, i = 1,\ldots,N \qquad \forall\, j = 1,\ldots,N$$

The number of the above connections is M, the size of the graph G.

2.3. Graph complexity reduction and sub-graph definition

The entire graph above described can be seen as an overlap of N different and independent sub-graphs. All sub-graphs have the same number of nodes (cards) of the G graph but each of them has a sub-set of connections of the original complete graph. Mathematically this partitioning operation can be formalized as follows:

$$\bigcup_{i=1}^{N} L_i = L \qquad \bigcap_{i=1}^{N} L_i = \{\phi\}$$

where L_i are N sub-sets of connections or sub-circuits. To figure out this partitioning operation, consider that each node has N overlapping layers and on each layer one set L_i of connections can be developed. In this way, all connections can be developed on different independent layers that guarantee no intersection between connections. With a new indexing k, the N sub-graphs are defined as follows:

$$G_k = (C,L_k) \qquad \forall\, k = 0,1,\ldots,N-1$$

Accordingly, graph G_0 is the loopback graph where each node is connected to itself. This full-coverage partition of the graph G provides interesting features. If the graph can be split into N sub-graphs then the entire optical interconnection circuit can be divided into N different, independent and simpler sub-circuits. Moreover, in every sub-graph, each node has only two connections instead of N, the outgoing (Tx) and the incoming (Rx) ones. These graphs are called *balanced digraphs*.

In summary, the original graph G with order N and size $M = N^2$ can be substituted with N simpler sub-graphs with order N and size $M_k = N$:

$$\begin{aligned} N_k &= order(G_k) = |C| = N \\ M_k &= size(G_k) = |L_k| = N \end{aligned} \qquad \forall\, k = 0,1,\ldots,N-1$$

2.4. Subgraph connection generation

In this section a method to generate the connections of all sub-graphs is presented, exploiting the circularity property. The connections are generated according to the following rule:

$$Sub\text{-}graph\ G_k = (C,L_k) \qquad \forall\, k = 0,\ldots,N-1$$

$$\ell_{i,j} = (c_i,c_j) \in L_k \qquad \forall\, i = 1,\ldots,N$$

$$\begin{cases} \text{if } (i + k) \neq N & j = \text{mod}(i + k,N) \\ \text{if } (i + k) = N & j = N \end{cases} \tag{1}$$

Index j wraps around after reaching card N. In this way, G_k is the graph which realizes the connections from cards i to cards $i + k$. Table 1 shows all sub-graphs connections generated with the incremental rule presented above for the case $N = 8$.

2.5. Subgraph connection and layout

In ICT apparatus an array of N cards is placed into the rack slots and connected to the backplane. The distance (*pitch p*) between cards is defined by design criteria such as component size, mechanical stiffness,

Table 1
Connection of sub-graphs.

k	Description	Connections	Index
0	Each card is connected to itself	$L_0 = \{(c_1,c_1),\ldots,(c_8,c_8)\}$	0 (Loopback)
1	Each card i is circularly connected to card j = i + 1	$L_1 = \{(c_1,c_2), (c_2,c_3),\ldots, (c_8,c_1)\}$	+1
2	Each card i is circularly connected to card j = i + 2	$L_2 = \{(c_1,c_3), (c_2,c_4),\ldots, (c_8,c_2)\}$	+2
3	Each card i is circularly connected to card j = i + 3	$L_3 = \{(c_1,c_4), (c_2,c_5),\ldots, (c_8,c_3)\}$	+3
4	Each card i is circularly connected to card j = i + 4	$L_4 = \{(c_1,c_5), (c_2,c_6),\ldots, (c_8,c_4)\}$	+4
5	Each card i is circularly connected to card j = i + 5	$L_5 = \{(c_1,c_6), (c_2,c_7),\ldots, (c_8,c_5)\}$	+5
6	Each card i is circularly connected to card j = i + 6	$L_6 = \{(c_1,c_7), (c_2,c_8),\ldots, (c_8,c_6)\}$	+6
7	Each card i is circularly connected to card j = i + 7	$L_7 = \{(c_1,c_8), (c_2,c_1),\ldots, (c_8,c_7)\}$	+7