Engineering Science and Technology, an International Journal xxx (2018) xxx–xxx

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Contents lists available at ScienceDirect

Engineering Science and Technology, an International Journal

journal homepage: www.elsevier.com/locate/jestch

Full Length Article

Low power domino logic circuits in deep-submicron technology using CMOS

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ARTICLE INFO

Article history:
Received 26 November 2017
Revised 10 June 2018
Accepted 16 June 2018
Available online xxxx

Keywords:
CMOS
Dynamic
Domino
Footer

ABSTRACT

Leakage power and propagation delay are the two major challenges in designing CMOS VLSI circuits, in deep sub-micron technology. This paper proposes a novel technique: Foot Driven Stack Transistor Domino Logic (FDSTDL) for designing CMOS domino logic gates for the reduction in leakage power and improved noise performance. Two, four, eight and sixteen input OR gates are designed using existing and proposed techniques. These logic gates are simulated on the PTM 32 nm node using HSPICE (Level = 54) in CMOS technology at a clock frequency of 100 MHz. Simulation results are compared based on power consumption, propagation delay and unity noise gain. Simulation results show that proposed domino technique has a maximum power reduction of 59.47% as compared to the CSK-DL technique and maximum delay reduction of 44.6% as compared to the M-HSCD technique in CMOS technology.

1. Introduction

Wide fan-in dynamic logic gates are the preferred choice in large memories and high-speed processors due to high speed and smaller area characteristics as compared to static CMOS logic gates [20]. The domino logic achieves high speed due to their lower noise margin compared to the static CMOS logic. Low noise margin also implies an increased sensitivity of the domino logic circuits towards noise source. The noise immunity of domino logic circuits can be increased by downscaling the technology. However, this will increase the power consumption of the circuit. In order to reduce the power consumption, the supply voltage is scaled down. This increases the delay of the circuit. Therefore, to compensate for this delay, threshold voltage scaling is done along with supply voltage scaling. Reduction in threshold voltage increases the speed of the domino logic but decreases the noise immunity of the circuit due to increase in sub-threshold leakage current [1,2]. Scaling of technology reduces the thickness of gate oxide that causes an exponential increase in subthreshold and gate leakage current. This leakage current may discharge the precharge node of the domino circuits. Therefore, leakage currents, noise sources, and low threshold voltage degrade the performance of domino logic circuits at high frequencies [17].

The Average power consumption of a domino logic gate is given by the Equation [4]:

$$P_g = P_{short} + P_{switch} + P_{leakage} \quad (1)$$

where P_{short} is the short circuit power consumption due to the shorting of the supply and ground.

Pswitch is the power consumed due to charging and discharging of the load capacitance.

Pleakage is the power consumed due to the gate and sub-threshold leakage current.

To reduce various components of power consumption, device dimensions and supply voltage are scaled down. Scaling of device leads to an increase in the leakage current due to the unwanted Short Channel Effects (SCEs) [5,19,22]. These short channel effects reduce the effective channel length of the device, which in turn, reduces the threshold voltage of the device.

To reduce the power consumption in domino logic circuits, several techniques have been proposed in the previous papers [7,11,13]. All of these techniques are modified form of the basic Footerless Domino Logic (FLDL) [6] and Footed Domino Logic (FDL) [6]. In these techniques, additional P and N channel transistors and delay elements are used to reduce power consumption, propagation delay and to improve the noise immunity of the domino circuits. Section 2 discusses these techniques in detail. Section 4 compares these techniques in terms of the power consumption, propagation delay and unity noise gain. This paper proposes a new domino technique for designing high-speed, large fan-in gates

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Peer review under responsibility of Karabuk University.

https://doi.org/10.1016/j.jestch.2018.06.013
2215-0986/

in deep sub-micron technology. The proposed technique uses stacked transistors for reduction of leakage power and improvement in noise performance. In the proposed technique, the contention between the keeper and the evaluation network decreases that reduces power consumption and propagation delay. For large fan-in gates. the proposed circuit shows improvement in noise performance by more than 1.4× compared to the existing techniques.

This paper discusses existing Domino styles in Section 2. Section 3 describes the proposed logic design using CMOS technology. Section 4 compares the proposed circuit with existing domino styles. Section 5 concludes the paper.

2. Domino logic styles

For implementing high-speed and high-performance microprocessors, domino logic is preferred over other dynamic logic styles due to lesser area and low power requirements [23]. Domino logic uses only one PMOS transistor in Pull-Up Network (PUN) [19], thus reducing the area and the power consumption compared to dynamic CMOS logic that uses n (No. of inputs) PMOS transistors in PUN. Noise immunity of domino circuit degrades due to the excessive scaling of technology. In addition, subthreshold leakage and gate leakage currents are major challenges in domino circuit design [14].

First technique proposed for domino logic design was Footerless Domino Logic [6] (FLDL) as shown in Fig. 1. In this technique, when the clock is low during the precharge phase, the precharge transistor (P2) turns ON and dynamic node charges to supply voltage (VDD) through P2. When the clock becomes high in the evaluation phase, the output of the circuit changes according to the inputs applied in Pull-Down Network (PDN). At this time, keeper transistor turns ON and connects the dynamic node to supply. Thus, prevents any undesirable discharge of the dynamic node due to charge sharing problem of Pull-Down Network [8,9]. Therefore, increase in the size of keeper transistor improves the robustness of FLDL logic.

The keeper ratio [7,13] is given by:

$$K = \frac{W_{keep}}{W_{eval}} \tag{2}$$

where W_{keep} is the width of keeper transistor and W_{eval} is the width of evaluation transistors. Therefore, on increasing K, the robustness of the domino circuit increases with the increase in power consumption and propagation delay.

Fig. 2 shows the variation of power consumption in FLDL domino circuit with the increase in the size of the keeper. As the size of keeper increase, power consumption increases due to increased contention between the keeper and evaluation logic.

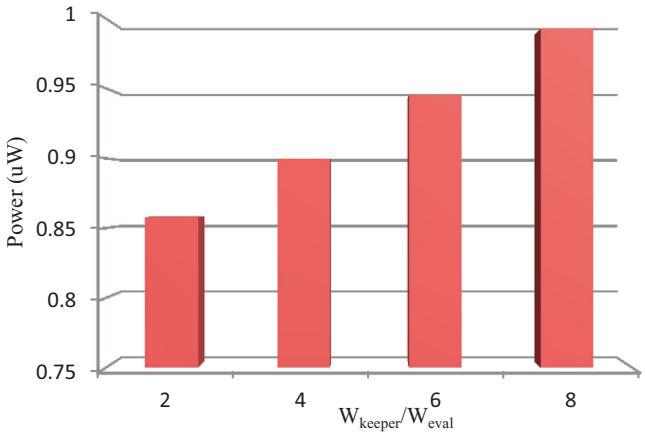

Fig. 2. Effect of keeper sizing on power consumption of FLDL domino logic circuit.

The major drawback of FLDL technique is that when all inputs are low during the evaluation phase, a leakage current flow through Pull-Down Network (PDN) due to subthreshold and gate tunnelling current. In Footed Domino Logic (FDL) [6,15] technique, this leakage current is reduced by inserting a footer transistor N1 in series with evaluation network as shown in the Fig. 3. The drawback of FDL technique is that footer transistor introduces a delay in the circuit that reduces the speed of the circuit. The Robustness of FDL decreases for high Fan-in gates [3].

To reduce the delay, current mirror transistors N2 and N3 are inserted in the FDL logic shown in Fig. 4. These transistors reduce delay but increase discharging current in the circuit. In order to stop discharging of the dynamic node, transistor N4 provides a feedback path from the gate of the current mirror to the output of circuit as shown in Fig. 4. When dynamic node discharges to the ground due to the presence of noise at the input, transistor N4 connects the gate of mirror transistors to ground. In evaluation mode, when the clock is high and all the inputs are low, the stacked transistors N1, N2 and transistors in evaluation logic decreases subthreshold current. In this way, the stacked transistor N2 improves noise immunity of the circuit. This technique is termed as Current Mirror Footed Domino (CMFD) [10] logic.

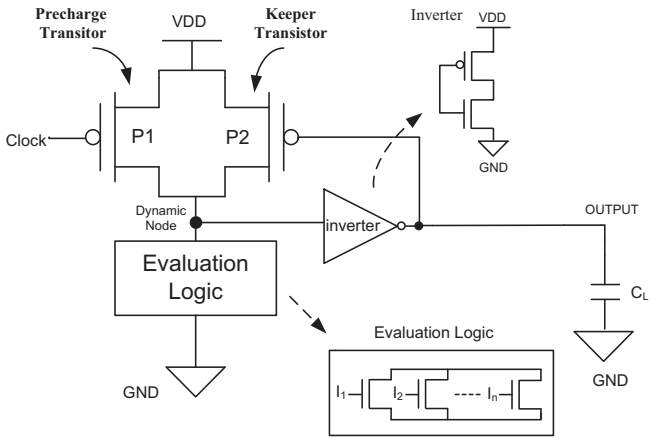

Fig. 1. Footerless Domino Logic (FLDL).

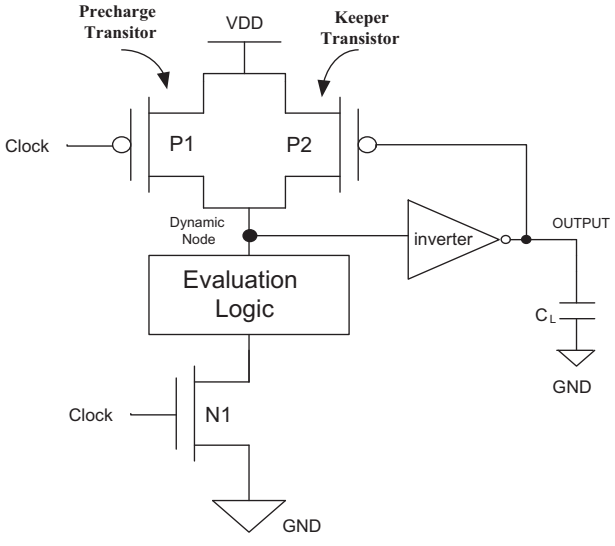

Fig. 3. Footed Domino Logic (FDL).

Please cite this article in press as: S. Garg, T.K. Gupta, Low power domino logic circuits in deep-submicron technology using CMOS, Eng. Sci. Tech., Int. J. (2018), https://doi.org/10.1016/j.jestch.2018.06.013