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Performance analysis of FPGA controlled four-leg DSTATCOM for multifarious load compensation in electric distribution system

Azhagesan Dheepanchakkravarthy^a, Syamalan Akhil^a, Kandadai Venkatraman^b,
Manickavasagam Parvathy Selvan^a, Sridharan Moorthi^{a,*}

^aHybrid Electrical Systems Laboratory, Department of Electrical and Electronics Engineering, National Institute of Technology, Tiruchirappalli 620015, India

^bDepartment of Electrical and Electronics Engineering, Vardhaman College of Engineering, Hyderabad, India

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ABSTRACT

A field programmable gate array (FPGA) controlled four-leg distribution static compensator (FL-DSTATCOM) has been implemented to achieve harmonic alleviation, supply current balancing, compensation of reactive power and current flow in the neutral conductor of a 4-wire 3-phase electric distribution system with static, dynamic and combined loads. The unbalanced non-linear and linear static loads are considered for analyzing compensation behaviour of FL-DSTATCOM. The practicability of FL-DSTATCOM for compensating reactive power under dynamic condition is evaluated with slip ring induction machine having variable load current. Also, the performance of FL-DSTATCOM is examined with combined load, which is a combination of dynamic and unbalanced static loads. The reference current signals are produced by using synchronous reference frame theory. Hysteresis band current controller is utilized for generating switching pulse for IGBT switches present in the FL-DSTATCOM. Independent modules are developed for realizing all the tasks in FPGA with the feasibility to reconfigure the hardware for any other application with similar requirements. The experimental results demonstrate that the FPGA controlled FL-DSTATCOM is capable of making the supply current as balanced and sinusoidal, maintaining the power factor at point of common coupling near to unity and reducing the supply neutral current very close to zero.

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1. Introduction

During power distribution, the 4-wire 3-phase electric distribution system (EDS) faces several issues on power quality (PQ) such as reactive, harmonic and neutral current flow and impermissible voltage drop owing to unbalanced non-linear/ linear loads [1]. These loads include electric arc furnaces, welding machines, computers, speed drivers in air conditioners, industrial pumps and other microprocessor based equipment, lighting load, house hold applications, laser printer, switched mode power supply, large uninterrupted power supply, boring machines, lathe, fans, refrigerators and so on. Similarly, the non-linear solid state converters are one of the major reason for injecting the harmonics into the EDS,

which affects the performance and leads to increased losses, poor efficiency and inadequate utilization of the EDS [2].

Various custom power devices (CPD) are addressed in [3] to enhance the quality of power in 4-wire 3-phase EDS. The power flow in the electric power distribution line could be effectively controlled with the help of ultimate CPD like distribution static compensator (DSTATCOM). The DSTATCOM is very attractive and it has a good cost-effective solution to minimize the PQ impact in EDS [4]. Various types of DSTATCOM topologies have been reported for neutral current compensation (NCC) and alleviating the PQ issues in EDS [5–7]. The split capacitor based three leg DSTATCOM, special transformer based DSTATCOM and four-leg distribution static compensator (FL-DSTATCOM) based topologies are broadly employed for NCC in systems with unbalanced/ balanced non-linear and linear loads. FL-DSTATCOM topology outweighed the others in terms of DC link voltage utilization and harmonic mitigation performance [5,8]. It has simple power circuit compared to other topologies and more control flexibility [9,10]. To ensure the PQ of the EDS, FL-DSTATCOM could be installed in between the supply and loads, at appropriate nodes.

* Corresponding author at: Hybrid Electrical Systems Laboratory, Department of Electrical and Electronics Engineering, NIT, Tiruchirappalli, Tamilnadu 620 015, India.

E-mail addresses: selvanmp@nitt.edu (M.P. Selvan), srimoorthi@nitt.edu (S. Moorthi).

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The digital implementation of control algorithm is essential to obtain a proper functioning of the FL-DSTATCOM. The advanced digital controllers like digital signal processors (DSPs), microprocessors, dSPACE and field-programmable gate arrays (FPGAs) are mostly preferred to implement digital controllers for solid state power converters. The capabilities of analog to digital converter (ADC), high processing power and more than required quantities of digital inputs/ outputs make these advanced control technologies a very attractive and effective selection for solid state power converters based applications.

Nowadays, the DSP and microprocessor are facing more complicating and fundamental challenge. These digital controllers have problems like delay in the calculation of the optimal switching state and parameters estimation. Additionally, they require high-frequency pulse width modulation and accurate voltage and current sensing [11,12]. The processing speed required to deal with this hardware-rich tasks reaches the order of microseconds to nanoseconds, as a result it becomes very complicated to implement within a DSPs or microprocessors software computation background. Additionally, the costs and complexity of these controllers are raised, due to the requirement of dedicated computers and specific integrated circuits. Similarly, dSPACE controller is also widely used in practice to achieve the control of power converters. Unfortunately it also has few drawbacks like need of additional software tools, requirement of dedicated computer and leads to high cost [13].

A hardware control solution using FPGA may solve the above problems. FPGAs are logic devices which contain a matrix of reconfigurable gate array logic circuitry. The use of FPGAs in low volume and high performance applications is very significant as it executes a lot of instructions in parallel which has lead them to be very powerful [14]. The main characteristic features of FPGAs are high processing speed, hardware programming flexibility and without changing the external circuitry, it is possible to reconfigure as per the requirement at a particular point of time [15]. These devices show greater potential for machine tool, solid state and deployed as controller for shunt/ series active filter, machine/ drive control, multilevel converters and chopper power circuits. Also, they are well-matched for manufacturing and automation environments [16].

The most attractive and highlighted feature in FPGAs is that they are programmed by utilizing Verilog HDL/VHDL (Hardware Description Languages (HDLs)) [17]. The advantage of using HDL is that it is technology independent and the software packages for these languages are freely available from Xilinx. The implementation of complex control designs on FPGAs is possible by defining hierarchical and modular description at various concept levels with the ultimate support of HDLs [13]. FPGAs utilize dedicated software and hardware for processing logic and it has a function of parallel processing, so they do not have a separate operating system [18]. A single FPGA controller is utilized to develop and implement the control algorithm for producing both low and high frequency switching pulses. The semiconductor switches available in hardware circuit is enabled by this switching pulses and to generate the preferred output signals [19].

Various current control methods are recommended for DSTATCOM configurations in the literature for generating the gate signals [20]. Based on that, hysteresis band current controller (HBCC) is highest efficient current control method compared to other current controllers. Owing to its advantages like high simplicity, good accuracy, outstanding robustness, fast dynamic response, current limiting capability and load time constant, it is mostly preferred and widely applied in DSTATCOM for compensating current related PQ problems. During the implementation it does not require complex processor. The switching pulses produced by HBCC module force the injected current to follow the reference compensator

current. The primary feature of the HBCC is that it estimates the current error signals and directly generates the reference commands to the semiconductor switches present in the FL-DSTATCOM, when the error signals exceeds an assigned hysteresis band [21].

This paper expresses that the FPGA control of FL-DSTATCOM can be successfully implemented to enhance the quality of power distributed to consumers through 3-phase 4-wire EDS. The compensation capability of FL-DSTATCOM is verified under static, dynamic and combined loading conditions. Under static loading condition, the performance of FL-DSTATCOM is tested with unbalanced non-linear and unbalanced linear loads. Under dynamic loading condition, slip ring induction machine (SRIM) is considered and it is operated as motor to explore the dynamic reactive power support capability of FL-DSTATCOM. In the combined loading condition, the parallel combination of unbalanced non-linear load with slip ring induction machine is tested for harmonic current alleviation, compensation of reactive power and supply neutral current. The $d-q-0$ components of load currents are utilized for generating compensator current for FL-DSTATCOM. The HBCC is utilized for producing the switching pulses required for eight semiconductor switches used in the FL-DSTATCOM. The various logic blocks of the synchronous reference frame theory (SRFT) control algorithm and HBCC has been programmed using Verilog HDL.

2. Implementation of FL-DSTATCOM and SRFT control algorithm

2.1. Experimental setup of FL-DSTATCOM

Fig. 1 shows the 3-phase power circuit schematic of FPGA controlled FL-DSTATCOM connected in a 4-wire 3-phase EDS. The laboratory prototype of FL-DSTATCOM is formed by connecting two 1-phase SEMIKRON make voltage source inverters (VSIs) (SKM150GB12T4) in parallel. In addition, SEMIKRON make 3000 $\mu\text{F}/450\text{ V}$ (SKC 3M2-45A-3) DC bus capacitor is connected across them. The FL-DSTATCOM, which is usually a current controlled inverter, achieves NCC by fourth leg with less DC bus capacitor and therefore achieving full utilization of voltage across the DC capacitor. Remaining three legs present in the FL-DSTATCOM are used to compensate the reactive power, improve the power factor (PF), reduce the current harmonic and regulate the voltage.

The midpoint of each leg is coupled to the EDS through the 10 mH, 10 kHz, Ferrite core interface inductors which are used for proper shaping of the compensator current. The harmonic and reactive parts of load current are provided by FL-DSTATCOM so that the supply current contributes to only the active part of load current. The FL-DSTATCOM is controlled dynamically to maintain the supply side PF at unity under static, dynamic and combined loading conditions by maintaining the required voltage across the DC capacitor.

2.2. FPGA implementation of SRFT and HBCC

Reference compensating signal extraction and command signal generation for the FL-DSTATCOM are important stages of the control algorithm. Control strategy is the primary part of FL-DSTATCOM which substantially affects compensation characteristics. In the literature [22–24], several control algorithms were described for extracting the reference signal of DSTATCOM. Due to its greater accuracy, the SRFT algorithm is provided to be the most superior one. In this work, SRFT based algorithm is implemented for constructing reference compensator current using FPGA controller. The basic building blocks of SRFT based control algorithm for compensating static, dynamic and combined loads in EDS is depicted in Fig. 2. Also, the schematic shown in Fig. 3 designates the modular description of the control algorithm which includes

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