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Full Length Article

A Discrete Event System approach to On-line Testing of digital circuits with measurement limitation

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ABSTRACT

In the present era of complex systems like avionics, industrial processes, electronic circuits, etc., on-the-fly or on-line fault detection is becoming necessary to provide uninterrupted services. Measurement limitation based fault detection schemes are applied to a wide range of systems because sensors cannot be deployed in all the locations from which measurements are required. This paper focuses towards On-Line Testing (OLT) of faults in digital electronic circuits under measurement limitation using the theory of discrete event systems. Most of the techniques presented in the literature on OLT of digital circuits have emphasized on keeping the scheme non-intrusive, low area overhead, high fault coverage, low detection latency etc. However, minimizing tap points (i.e., measurement limitation) of the circuit under test (CUT) by the on-line tester was not considered. Minimizing tap points reduces load on the CUT and this reduces the area overhead of the tester. However, reduction in tap points compromises fault coverage and detection latency. This work studies the effect of minimizing tap points on fault coverage, detection latency and area overhead. Results on ISCAS89 benchmark circuits illustrate that measurement limitation have minimal impact on fault coverage and detection latency but reduces the area overhead of the tester. Further, it was also found that for a given detection latency and fault coverage, area overhead of the proposed scheme is lower compared to other similar schemes reported in the literature.

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1. Introduction

With the advancement of technology and larger scales of production, intelligent automation systems are increasingly making their presence felt in all aspects of engineering such as avionics, industrial processes, manufacturing systems, transportation systems, electronic systems, etc.[1,2]. Due to the increase in complexity of these systems, there is also a rise in the number of faults occurring in them. Such systems are required to be always available when needed and maintained on the basis of their current condition monitoring, rather than scheduled or breakdown maintenance [3,4]. In other words, the classical philosophy of performing burn-in tests after production and deploying the system with the assumption of fault free behavior thereafter may not be valid. So, On-line Testing (OLT) i.e., on-line fault detection is becoming an indispensable part of testing [5–8].

Several approaches to on-line fault detection have been reported in the literature and can be broadly classified as fault-tree based analysis [9], expert system based methods [10], machine learning techniques [11,12] and model based methods [13–15]. Any kind of automated reasoning, ranging from fault detection to stability analysis of complex systems, can be achieved efficiently through model based representations. In a model based approach, a detailed process model is constructed first. The system states are estimated from this model and the corresponding fault condition is determined based on the values of the measurable system parameters. The commonly used model based techniques are analytical redundancy based methods [16], Discrete Event System (DES) model based methods [13–15], Hybrid System (HS) model based methods [17,18], etc. DES model based methods are used for fault detection for a wide range of applications because of simplicity of both the model and the associated algorithms. Further, most systems, even with continuous dynamics, can be viewed as DESs at some level of abstraction. A DES is characterized by a discrete state space and some event driven dynamics. The core idea is to develop the normal and faulty DES models corresponding to normal and abnormal scenarios of the system. Subsequently, a detector which is a state estimator is built that determines whether the system is operating under normal, fault or uncertain conditions.

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One of the major infrastructure involved in DES based fault detection is sensors that measure the system parameters continuously, which in turn are used by the detector [19–21]. The more the number of parameters that can be measured by the sensors and given as input to the detector, the higher is the number of faults that can be detected. However, many factors like cost, physical conditions involving extremely high temperature, etc. limit the feasibility of deploying sensors in all the required points in the system. So, instead of measuring all parameters, a subset of parameters are measured and fault detection is performed by the detector only based on such measurements [20,21]. Thus, fault detection under limitation on measuring system parameters i.e., measurement limitation is an important area of research [20,21].

In VLSI circuits, fault detection is one of the major challenges to achieve acceptable quality of service [22]. Moore had predicted in his seminal paper [23] that transistor density of VLSI circuits would double every 18 months. The prediction has proved to be correct and at present we have reached the Deep Submicron (DSM) era, where single chip implementation of complex systems, network of processor cores, etc. have been successfully fabricated. DSM VLSI circuits involve millions of transistors on a single chip and the operation speed is at the level of GHz.; such high complexity of fabrication also increases the possibility of faults in the fabricated chips [22,24]. Traditional testing schemes like Automatic Test Equipment (ATE) based testing, Built in Self Test (BIST), etc. cannot detect many of these faults. ATE based testing, also called manufacturing test involves connecting the fabricated chip to the tester, applying test patterns and comparing with golden response [25,22]. In BIST, every time before powering up the circuit it is tested using on-chip pattern generator and response analyzer [26]. However, in DSM circuits probability of development of faults during operation is also being observed frequently [27–29]. To elaborate, such faults were not present during manufacturing or during powering up of the circuit, but developed on-the fly during its operation. So classical manufacturing test and BIST cannot detect faults that occur during operation of the circuit. To detect these faults that develop on the fly, a new test methodology called On-Line Testing (OLT) is required. *OLT of circuits can be defined as the procedure to enable integrated circuits to verify the correctness of their functionality during normal operation by checking whether the response of the circuit conforms to its desired dynamic behavior.* OLT for digital circuits is being studied for the last two decades and can be broadly classified into the following main categories, (i) Signature monitoring in Finite State Machines (FSMs) [30,31], (ii) Self-checking design[28,32,33], (iii) Partial replication [34–36]. (iv)On-line Built-in-Self-Test (BIST) [37–39]. OLT techniques have emphasized on keeping the schemes as non-intrusive as possible (i.e., minimal change to the original circuit), totally self-checking, low area overhead, high fault coverage (mainly single stuck at faults), low detection latency etc. However, in the DSM era, several other factors need to considered for OLT namely, coverage for advanced fault models (e.g., bridging faults, delay faults etc.), scalability, flexibility of area overhead of the tester versus fault coverage and detection latency etc. Some important contributions in this area are [27,40,35,36].

The on-line tester circuitry executes concurrently with the CUT and needs to tap certain lines of the CUT. These tap points can be considered as sensors for the tester. As the on-line tester is fabricated on the same chip with the CUT, any point of the CUT can be tapped. This enables the measurement of any required digital parameter of the CUT by the tester. So, most the above mentioned OLT techniques have ignored the issue of tap points or measurement limitation. However, tapping of lines of any circuit results in increase of load (fanouts) on the gates which drive the tap points [41]. To handle the increased load extra buffers are required, which increase the area of the circuit. So if the on-line tester is designed with high number of tapings in the CUT, it results in huge area overhead. So, in this work we aim at design of on-line testers for digital circuits, targeting minimization of tap points using the concept of DES based fault detection with measurement limitation. However, reduction in tap points also compromises fault coverage and detection latency. Therefore, "number of tap points" can be used as parameter to tradeoff area overhead versus fault coverage and detection latency.

In this paper, we propose a DES based scheme for design of on-line testers of digital circuits, targeting minimization of the number of tap points subject to fault coverage and detection latency. Most of the operations for construction of the on-line tester are based on Ordered Binary Decision Diagrams (OBDDs) [42]. OBDDs represent Boolean functions in a compressed form. Further in OBDDs, operations can be performed directly on the compressed representation, i.e., without decompression. So complexity of the on-line tester design is greatly improved by using OBDDs compared to traditional data structures like Binary tree, FSM etc. The time complexity of designing the on-line tester is also discussed in this paper. Experimental results on ISCAS89 benchmarks have been presented, which illustrate that measurement limitation can be used as a tradeoff parameter to minimize area overhead to a great extent, with minimal compromise in detection latency and coverage. It was also found that for a given detection latency and coverage, area overhead of the proposed scheme is lower compared to other similar schemes reported in the literature.

The paper is organized as follows. In Section 2 we start with literature review on OLT followed by motivations and contributions of the present work. Section 3 presents state based DES modeling and *FN*-detector construction under measurement limitation. Section 4 illustrates use of OBDDs to generate *FN*-detector efficiently. The complexity of construction of the *FN*-detector is also discussed in this section. Section 5 presents experiential results regarding area overhead, fault coverage and detection latency versus measurement limitation (i.e., tap point reduction) of the *FN*-detector. Finally we conclude in Section 6.

2. Literature review and motivation of the work

In this section we briefly discuss the major contributions related to OLT of digital circuits and then build the motivation of the present work. As already mentioned, OLT techniques for digital circuits can be broadly classified into (i) signature monitoring in FSMs, (ii) self-checking design, (iii) partial replication and (iv) on-line BIST.

Signature monitoring in FSMs: Signature monitoring techniques for OLT (of sequential circuits) work by modeling a circuit as FSM and studying the state sequences during its operation. The basic assumption is signature invariant property i.e., signature of a circuit, obtained based on state sequence, is different under normal and faulty conditions. The feasibility of signature invariance is proved in [43] and several authors have proposed implementations based on this approach [44,30,31]. The hybrid signature monitoring scheme reported in [30] detects control flow errors caused by transient and intermittent faults. It is shown that the scheme has offered very high fault coverage with low detection latency and area overhead. In [31], a concurrent control flow error detection and recovery mechanism has been proposed using encoded signature monitoring technique. The scheme recovers from most of the control flow errors with relatively low performance overhead.

However, many times by default, signature invariance is not present. In that case, redundant states need to be inserted and state encoding is modified. So these schemes require re-synthesis and re-design, which lead to a change in the original structure of the circuit; they are accordingly termed as "intrusive OLT methodolo-

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