ARTICLE IN PRESS

Engineering Science and Technology, an International Journal xxx (2016) xxx–xxx

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Contents lists available at ScienceDirect

Engineering Science and Technology, an International Journal

journal homepage: www.elsevier.com/locate/jestch

JESTECH

Review

Spintronics: A contemporary review of emerging electronics devices

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A R T I C L E I N F O

Article history:
Received 19 August 2015
Revised 2 May 2016
Accepted 2 May 2016
Available online xxxx

Keywords:
Spin valve
GMR
MTJ
FTJ
Spin-FET
Spin-MOSFET

A B S T R A C T

Spintronics is a new field of research exploiting the influence of electron spin on the electrical conduction (or current is spin dependent). The major problem is the realization and fabrication of spintronics based devices. To meet the objective scientific community is developing the novel kind of materials that relies on magnetism instead of flow of current through electron. This paper illustrates and reviews one of the emerging technologies known as spintronics by putting few low power computing techniques altogether based on spintronics to provide a basic and meaningful understanding to the reader. The challenges of spintronics devices that has to meet for the success of electronics future are summarized.

Contents

1. Introduction

As the channel length is keep on reducing, downsizing the channel length has become a major concern [1]. The expected gate length in future is 5 nm, because of that, off leakage current will be too high for the entire chip (ITRS map 2008) [2]. However, there are various techniques to reduce the off chip power in which double gate-metal oxide semiconductor field effect transistor (DG-MOSFET), fin-field effect transistor (fin-FET) and Si-nanowire MOSFET are the most promising one [3]. Dual material surrounding gate (DMSG) MOSFET is also another approach to improve the carrier transport efficiency and reduce the short channel effects by employing gate material engineering [4]. Carbon nanotube field effect transistor (CNTFET) is another feasible nanodevice similar

http://dx.doi.org/10.1016/j.jestch.2016.05.002
2215-0986/

Please cite this article in press as: V.K. Joshi, Spintronics: A contemporary review of emerging electronics devices, Eng. Sci. Tech., Int. J. (2016), http://dx.doi.org/10.1016/j.jestch.2016.05.002

in structure and successor of complementary metal oxide semiconductor (CMOS) technology. It has higher performance, transconductance and lower power consumption etc. than conventional CMOS technology. A lot of logics have been developed using these methods [5]. The problem with all above mentioned logics are volatility. Spin logics are the emerging one, which improves the battery life by consuming less power from portable devices to large data centers [6] and are non-volatile in nature.

Two diversified field of low power spintronics technologies are the active and passive devices. Here, few low power spintronics technologies of active devices like spin valve, giant magneto resistance (GMR), magnetic tunnel junction (MTJ), ferroelectric tunnel junction (FTJ) and domain wall (DW) in magnetic nanowires have been discussed. The other two domains of technologies under passive devices are monolithic and hybrid technologies. In monolithic spintronics the data storage and data communication is done by spin only (for example single spin logic (SSL)). SSL is a novel type of computer technology proposed in 1994 and popular due to bi-stable spin states of the electrons in quantum dots. This technology forms the SSL using quantum dots, magnetic field and electrons altogether. To understand the monolithic technologies one example of SSL, a universal logic NAND gate and its realization is discussed. In hybrid spintronics the data storage and data communication is done by charge only (either electron or hole), but its effect is augmented by the presence of spin. Spin plays a secondary role and influences how charge stores or manipulate information [7]. It has been shown in the literature that hybrid spintronics do not really show the significant advantages over the traditional bipolar junction transistor (BJT) or MOSFET based transistor [8]. The reason for that, the logic '0' or logic '1' is still decided whether the transistor is on or off. If the current flows from drain (D) to source (S) logic '1', or if no current logic '0' will be considered. To understand the hybrid technologies, an example of theoretically developed spin-FET and spin-MOSFET is addressed. In spin-MOSFET, graphene is used due to its low spin orbit interaction in the channel region which has shown interesting effects on conventional electronics. It has opened the way of "beyond CMOS" to develop the spin only logic circuits. These circuits consume less power than conventional CMOS.

Spintronics is one of the emerging technology which has extended the Moore's law and industry is trying to put more than Moore. Any technology can replace the current world of electronics if it reduces any one of the very large scale integration (VLSI) cost functions like area, power consumption and speed etc. Fortunately, spintronics can reduce heat dissipation significantly. In charge based device to switch from logic '0' to logic '1' the magnitude of the charge must be changed in the active region of the device due to which current flows from S to D. It is not possible with charge based electronics to reduce the power (or heat) dissipation, since charge is a scalar quantity and the presence or absence of charge gives logic '1' or logic '0'.

Spin unlike charge is a pseudo vector quantity which has a fixed magnitude of $h/4\pi$ with a variable polarization. If an electron is placed in magnetic field it can have more than two states but in digital only two bits 0 and 1 can be encoded, rest all cases are not required here and only these two states will have eigen states. These states can be achieved with a polarization parallel and antiparallel to the field which encode logic 1 and logic 0 respectively. In that case switching is accomplished by flipping the polarization of spin without any change in flow of current as that was the case in hybrid spintronics. This may result in significant energy saving. However, there is still some energy dissipated in flipping the spin but it will be of the order of $g\mu_B B$, where g is Lande factor, μ_B is the Bohr magnetron and B is the magnetic field required to keep the spin polarization bistable. The term $g\mu_B B$ can be reduced by lowering B, but it may cause more random bit flips. However, bit flip errors can be handled up to an extent by error correcting codes up to a certain extent [9,10].

To understand the charge particle behavior in metal, first I would like to discuss the relation between energy and density of states of metal. The spin polarization has been calculated theoretically by the below given relation [7,11,12],

$$P_n = \frac{n_\uparrow - n_\downarrow}{n_\uparrow + n_\downarrow} \quad (1)$$

If $n_\downarrow = 0$; $P_n = 1$ in this case only majority spins are there and the spin polarization is 100%. Such materials are known as ferromagnetic half metals or heusler alloys with 100% spin polarization. Heusler alloys (or half metals) are ferromagnetic metal alloys based on a heusler phase [13]. One example of half metals is strontium doped lanthanum manganate (LSMO), well known for its colossal magneto resistive behavior and has 100% spin polarization at low temperature (0 K), but it is difficult to achieve 100% spin polarization for spintronics devices and a lot of argument are there in the literature [14]. LSMO materials also show a sharp transition from metal to insulator at transition temperature. If $n_\uparrow = 0$; $P_n = -1$, if $n_\uparrow = n_\downarrow$; $P_n = 0$ (only for paramagnetic or normal metal). These three cases has been shown in Fig. 1, using Stoner-Wohlfarth (SW) model of ferromagnet [15,16]. Later people used this simplest SW model and did further modification to understand the physics of magnetization of digital magnetic storage like floppies, hard disk and magnetic tapes. The E-K diagram has been shown in Fig. 2. The up (↑) and down (↓) spins related energy is calculated by the Eq. (2) or (3) [7],

$$E_\uparrow = \frac{h^2}{4\pi^2 m_0} K^2 \quad (2)$$

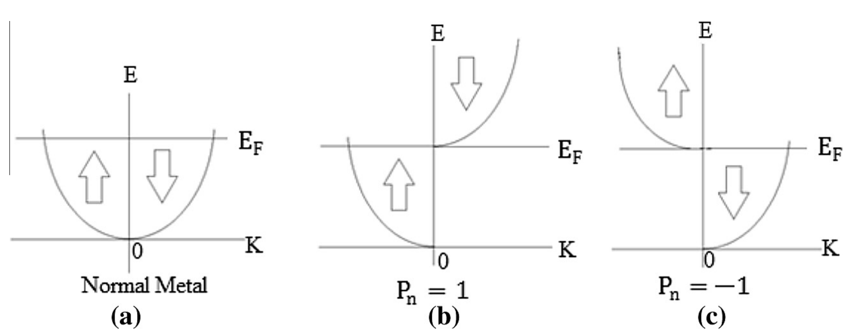

Fig. 1. Energy level (E-K) diagram using SW model (a) In normal metal both up spin and down spin are equal (b) if $n_\downarrow = 0$, and $n_\uparrow$ is 100% spin polarized has $P_n = 1$ (c) here $n_\uparrow = 0$, and $n_\downarrow$ is 100% spin polarized has $P_n = -1$ [11,12].

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