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ScienceDirect

Procedia Computer Science 115 (2017) 756–763

Procedia Computer Science

www.elsevier.com/locate/procedia

7th International Conference on Advances in Computing & Communications, ICACC-2017, 22-24 August 2017, Cochin, India

New Modified Current Starved Ring Voltage Controlled Oscillator and Frequency to Voltage Rectifier for Noise Suppression from 1 – 6 GHz in 180 nm Technology

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Abstract

This paper proposes a new and simple combined effort of a NMOS sink current starved ring voltage controlled oscillator (NS-CSRVCO) fed-back with a manual frequency to voltage rectifier (FVR) for noise suppression in mixed signal applications. The VCO and FVR operate from 1-6 GHz, with the VCO providing a tuning range of 176.4% with excellent linearity in oscillation frequencies from 0.3444 GHz – 5.679 GHz with a center frequency of 3.024 GHz, within a control voltage (VDD) of 0.6 V to 2.5 V. The properties of both the VCO and FVR makes it suitable for Military, Satellite applications in the microwave range.

Peer-review under responsibility of the scientific committee of the 7th International Conference on Advances in Computing & Communications.

Keywords: NS-CSRVCO; FVR; linearity; wide tuning range; ultra-low power; low die area; low ac ripples; noise suppression

1. Introduction

Voltage Controlled Oscillators (VCOs) and Frequency to Voltage Rectifiers (FVRs) form important parts of a Phase Locked Loop (PLL), ring oscillators et al. An ideal VCO/FVR is one whose output frequency/voltage is a

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1877-0509
Peer-review under responsibility of the scientific committee of the 7th International Conference on Advances in Computing & Communications
10.1016/j.procs.2017.09.170

linear function of the applied input voltage/frequency. In addition to this the VCO and FVR must be: operating over a wide frequency range, consume ultra-low power and be compact in size. For the jitter to not move around in PLL design, a VCO with linear gain must be used, the FVR used must be fast with low ac output ripples.
With an explosive growth in wireless communication technologies; the demand for low power, compact size, wide tuning range VCOs and FVRs have increased over the years [1-6]. CMOS technologies with low feature size have become attractive for realizing compact, ultra-low power, high frequency ICs [7]. VCOs are realized by LC resonant circuits or ring oscillators. LC oscillators have better phase noise and provide high output frequency, but with a low tuning range. On the other hand, CMOS ring oscillators provide: wide tuning range, low power consumption, and require low die area but require higher number of stages [8-11].
FVRs are designed by low-pass filtering of fixed time period pulses over time, counting number of pulses, and integration of fixed width pulses. Approaches such as parallel path signal division [12, 13] and capacitance charge redistribution [14, 15] have been published for FVR design. A low-pass filter is usually connected for the reduction of ac ripples in the output of the FVR. Although, CMOS Ring Oscillators have the above said advantages, they require increased number of stages for higher frequency of operation. This leads to higher power consumption, larger die area requirement, high design complexity and narrow operating bandwidth. CMOS Ring Oscillators are pushed towards high level of integration/density by Current Starved Ring (CSR) VCOs which exhibit wide tuning range and achieve a practical balance among area, power and phase noise [16, 17]. Past works on CMOS or non-CMOS ring oscillators using 180nm technology shows wide tuning range with high power consumed, or low tuning range with high power consumed, high phase noise and large number of stages [16-26]. Similarly, FVRs designed use complex circuitry, consume high power and use large die area for CMOS integrated applications. These increase the design complexity and cost of the circuit designed.
In this work, we propose a new and simple three stage NMOS Sink Current Starved Ring Voltage Controlled Oscillator (NS-CSRVCO) using NMOS sinks instead of sources and current mirrors for inverter starving. The FVR is a simple rectifier with a NMOS switch fed with square waves of appropriate frequency and amplitude, a diode using a NMOS transistor and attached to a suitable capacitor. The VCO and FVR are both designed using TSMC 180nm parameters and simulated using AWR v.12. The rest of the paper is structured as follows: Section 2 describes the circuit design procedure and operation of the proposed NS-CSRVCO and FVR while section 3 discusses about the simulation results, section 4 discusses about noise suppression using the proposed FVR and section 5 details the conclusions and future work.

2. Operation and Circuit Architecture of the NS-CSRVCO and FVR

This section explains in detail both the operation and design procedure of the NS-CSRVCO and FVR. Both of them are designed and implemented using MOSIS 180 nm parameters. The ring oscillator works by charging and discharging the gate capacitance of the MOSFETS of each inverter. Increasing the peak current takes less time for the capacitor to charge to the peak point. Consequently, the frequency of operation is increased. The manual FVR operates by charging three capacitances namely: the gate oxide, the drain source and the 1 pF capacitors. It is to be kept in mind that the NMOS switch used for the FVR must always operate in the linear region to be used as a resistor. Hence, the amplitude at the drain is manually controlled for linear (Ohm's region) operation of the NMOS and the FVR acts as a simple RDC (Resistor Diode Capacitor) rectifier.

2.1. Design of New NMOS Sink – Current Starved Ring Voltage Controlled Oscillator (NS-CSRVCO)

A normal ring oscillator works by feeding the output of the nth stage (odd) inverter to its input. Ring oscillators can generate very high frequencies upto 10 GHz and can withstand process and temperature variations. A control voltage is used to control the current and thus the delay of each inverter of the ring oscillator. An assumption that a propagation delay (T_{pd}) with each inverter and a logic level propagating around the loop in the absence of a stable D.C. point is made, which results in one inversion around the loop. Each delay element provides a phase shift of π/n and the remaining phase shift of $(2\pi-(\pi/n))$ is provided by the D.C. inversion. A detailed delay analysis of a basic current starved ring oscillator is done here [27]. The oscillation period is thus twice of the propagation delay (T_{pd}) around the loop. Hence, the oscillation frequency can be expressed as (1).