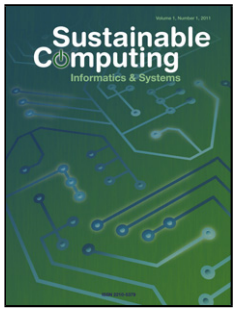

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High-Performance and Energy-Efficient Fault-Tolerance Core Mapping in NoC

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Abstract

Network on Chip (NoC) has been proposed as an efficient solution to communication problems in on-chip processors. The probability of failure increases in these systems because the complexity involved in continuous device scaling and the number of components embedded on a chip increases. Therefore, a fault-tolerant design has become a key aspect of designing chips to enhance the system reliability. This paper proposes a system-level mapping technique called FTCM, which enhances the performance and communication energy. It emphasizes on core mapping based on the application core graph and spare core placement in non faulty available processing cores because of core failures in the NoC. This technique mainly focuses on the issue of spare core allocation and its impact on the system performance. Experimental results shows that the communication energy conservation in FTCM is 16.8% compared with FASA and 19.2% compared with FARM, performance improvement of FTCM is 12.6% compared with FASA and 14.77% compared with FARM. Moreover, our method is applicable to both random and distributed core graphs.

Keywords: Network on Chip (NoC), core, fault tolerance, spare placement, System on Chip (SoC).