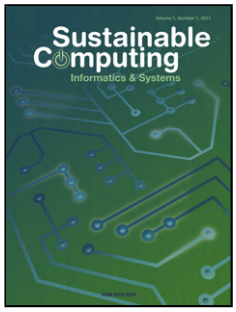

Title: P^{2}NoC: Power- and Performance-aware NoC Architectures for Sustainable Computing

Authors: Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore, Sujay Deb

PII: S2210-5379(16)30230-X
DOI: http://dx.doi.org/10.1016/j.suscom.2017.08.005
Reference: SUSCOM 182

To appear in:

Received date: 9-12-2016
Revised date: 17-7-2017
Accepted date: 23-8-2017

Please cite this article as: Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore, Sujay Deb, P2NoC: Power- and Performance-aware NoC Architectures for Sustainable Computing, Sustainable Computing: Informatics and Systemshttp://dx.doi.org/10.1016/j.suscom.2017.08.005

P²NoC: Power- and Performance-aware NoC Architectures for Sustainable Computing

Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore, and Sujay Deb
Department of Electronics and Communication Engineering, Indraprastha Institute of Information Technology, Delhi, India

Highlights

The Highlights of the paper are:

- **A two-step hybrid methodology for estimating router utilization with low runtime overheads.**
- **Implementation of Power and Performance Network-on-Chip (P2NoC) router architecture with power management controller to apply fine grained power gating in NoC routers and WIs for designing sustainable computing platforms.**
- **Design of router bypass links and control circuitry to transfer data through power gated routers.**
- **A deadlock free seamless bypass routing strategy for P2NoC, that makes use of bypass links to minimize adverse effects of power gating and maintain performance**

Abstract

—Communication performance over distant nodes and high power consumption are major challenges for efficient Network-on-Chip (NoC) architectures. Wireless NoCs, by augmenting wired topologies with low latency wireless links, overcome performance limitations of conventional NoCs. However, NoC routers and Wireless Interfaces (WIs) consume significant amount of leakage power. The usage of routers in NoC is application dependent and for most applications, performance requirement can be achieved without operating all resources all the time. Similarly, WIs transmitting data over shared channel can be selectively turned off when they are not active. Exploiting these, we propose Power- and Performance-aware NoC (P²NoC) architecture that power gates router elements and WIs depending upon their utilization to reduce leakage power. P²NoC works based on hybrid two-level router utilization estimate; pre-computed and runtime to provide coarse and fine estimate of utilization to maximize power saving while keeping overheads and performance impact to a minimum. We also propose deadlock-free seamless bypass routing strategy with P²NoC to avoid adverse impacts of power gating. P²NoC saves up to 92.20% and 68.23% of leakage power in base and hybrid routers respectively with only 7% area overhead. Based on utilization, P²NoC also reduces total average packet energy consumption by 49% with negligible performance degradation. The proposed solution provides a flexible sustainable computing platform that can be optimized for a wide range of application scenarios.