



IGZO TFT gate driver circuit with large threshold voltage margin[☆]

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ABSTRACT

This paper proposes a new gate driver circuit using depletion mode a-IGZO TFTs. The proposed gate driver circuit can prevent Q node, the gate node of pull-up TFT, from discharging during the output pulse duration. For that purpose, our circuit applies sufficient negative gate-to-source bias (V_{gs}) to the switch TFTs connected to the Q node during that time. Consequently, the leakage current through them is suppressed even though they have a negative threshold voltage (V_{th}). The proposed circuit has eleven transistors and two capacitors and it requires only two clock signals, which enables us to adopt the circuit at minimum extra cost. It works properly even when V_{th} is as low as -7.1 V. The normalized power consumption of the proposed circuit is also lowered compared with the previously reported circuits when the transistor has negative V_{th} . The power consumption of the proposed circuit for V_{th} of -5 V increases only nine times that for V_{th} of 3 V.

1. Introduction

Amorphous indium gallium zinc oxide thin film transistors (a-IGZO TFTs) have become a suitable candidate for various flat-panel displays due to high mobility and uniform electrical properties as compared to amorphous Si:H [1–3]. Due to the high mobility of a-IGZO TFTs, the active matrix liquid crystal displays (AMLCDs) using a-IGZO TFTs are able to provide high frame frequency and high resolution. The a-IGZO TFTs are also used for the backplane of active matrix organic light emitting diode (AMOLED) displays. However, the a-IGZO TFTs have a problem of negative threshold voltage [4–10]. The leakage current through these TFTs in a conventional gate driver circuit induces anomalously large power consumption [11–13]. Therefore, studies for the gate driver circuit that can be operated in the depletion mode would be useful for a-IGZO TFT display [14]. In this paper, we present a new gate driver using depletion mode a-IGZO TFTs. The proposed gate driver circuit can prevent the discharging of Q node, the gate node of pull-up TFT, for the output pulse duration. Negative V_{gs} is applied to the switch TFTs connected to the Q node during that time so as to prevent the leakage current through them even though they have a negative V_{th} . The proposed circuit has a very simple structure compared to those in previously reported papers. The proposed circuit has large V_{th} margin for circuit operation. The normalized power consumption of the proposed circuit decreases as the V_{th} increases in the negative direction, when compared with gate driver circuits in previously reported papers.

2. Proposed gate driver circuit and operation

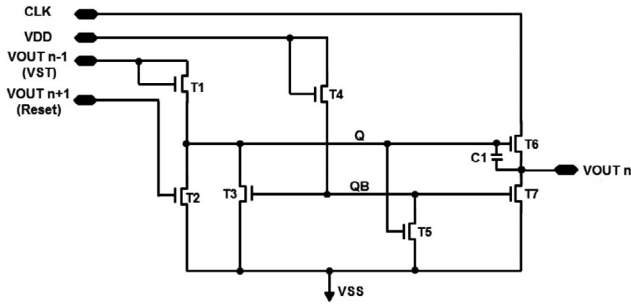
2.1. Problems of conventional gate driver circuit

The conventional gate driver circuit using depletion mode a-IGZO TFT has two problems. The first problem is the voltage drop of Q node during the output pulse duration. Whenever this phenomenon gets severe, the gate driver circuit does not work. To be more specific, during the pre-charging and the output pulse durations in a conventional circuit (Fig. 1), the QB node has very low voltage level (VSS) and the value of V_{gs} of T3 transistor is close to zero. If the conventional circuit has depletion mode TFTs, T3 transistor is not completely turned off. As a result, a considerable amount of leakage current flows through. The second problem is high power consumption due to the leakage current of the inverter circuit composed of T4 and T5 transistors that control the QB node. In the holding duration, the root mean square (RMS) value of the low Q node voltage is about -4.95 V. Thus, the V_{gs} of T5 transistor is set to about 0.05 V based on RMS voltage of Q node. The charge in the QB node is discharged to the VSS node by the T5 transistor in an unusually turned on state. The QB node is then charged from the VDD node by T4 transistor. Thus, the power consumption of the conventional gate driver circuit sharply increases as negative V_{th} increases due to the leakage current of the inverter circuit. This phenomenon also occurs in the circuits in previously published papers [3,12].

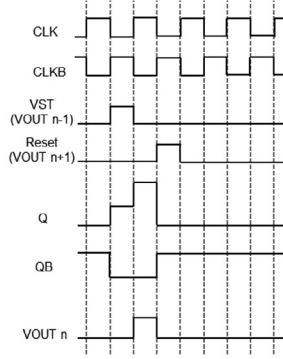
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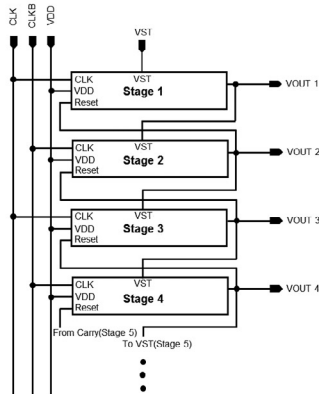
E-mail addresses: keechan@konkuk.ac.kr (K. Park), yongsang@skku.edu (Y.-S. Kim).



(a)



(b)

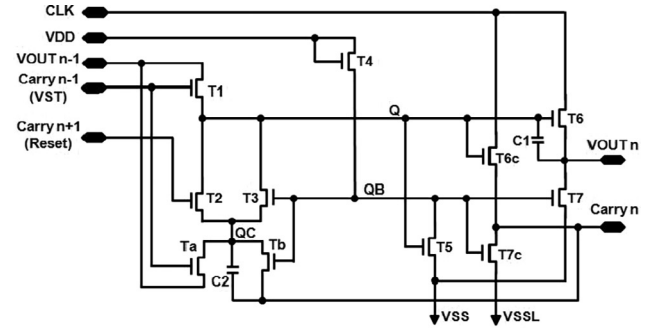


(c)

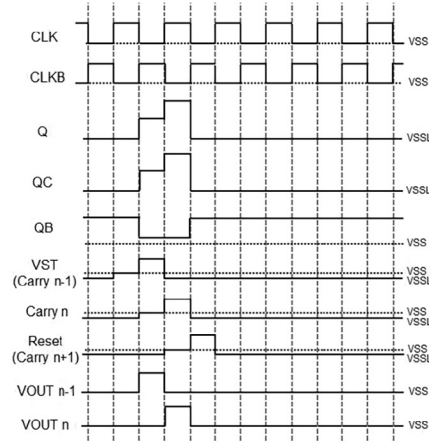
Fig. 1. The conventional gate driver circuit: (a) 1 stage circuit unit, (b) timing diagram, and (c) block diagram.

2.2. Proposed gate driver circuit

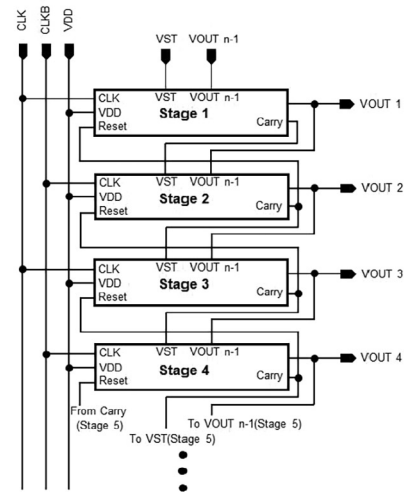
Fig. 2 shows the proposed depletion mode a-IGZO TFT gate driver circuit, timing diagram, and block diagram. The 1 stage unit of the proposed circuit is composed of eleven transistors and two capacitors as shown in Fig. 2(a). The circuit has two clock signals, namely CLK and CLKB. Three sources of DC voltages are applied to this circuit: VSS of -5 V, VSSL of -13 V, and VDD of 28 V. It has three operation durations: pre-charging duration, output pulse duration, and holding duration. We have proposed two new concepts in this circuit. According to the first concept, the circuit introduces a new node called QC, as shown in Fig. 2(a) and (b). In the circuit, the discharging of the Q node caused by the leakage current of T2 and T3 transistors during the output pulse duration can be prevented due to the addition of QC node. In [12], it is



(a)



(b)



(c)

Fig. 2. The proposed gate driver circuit: (a) 1 stage circuit unit, (b) timing diagram, and (c) block diagram.

reported that a similar QC node can be charged to the VDD node and discharged to the VSSL node using transistor switching. This circuit path is a leakage current path, accompanied by a consequent power consumption increase. However, the QC node of our proposed circuit is charged by Ta transistor, boosted by the C2 capacitor, and discharged by Tb transistor. Thus, our circuit has no leakage current path. In the

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