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Contention free delayed keeper for high density large signal sensing memory compiler

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ABSTRACT

Compiler based embedded memory is essential for SoC design. A new Contention Free Delayed Keeper (CFDK) topology has been developed in a leading edge 14 nm System-on-Chip (SoC) technology to improve the read performance of register file (RF) memories which can be easily used for both high density (HD) and high performance (HP) RF memory compiler design. This technique never allows contention and this helps to improve V_{min} (minimum operating voltage at which design is functional) significantly compared to a conventional keeper with low area overhead. It does not require fine tuning the keeper delay across the range of the local bit line (LBL) lengths that the compiler supports. It is shown that the proposed technique enhances the circuit evaluation speed by at least 68% while reducing power dissipation by 2.75% as compared to conventional domino logic. It also shows minimum 10% improvement in area with at par or better V_{min} and performance over other delayed keeper techniques. The same technique can be broadly applied to any domino path design including ROM design.

1. Introduction

Embedded memory requirements can span a large range of different size of memory instances depending on the application. For performance driven computational applications we need memories [1–3] which can operate at reasonable supply voltage (V_{min}) with high speed. In consumer mobile applications high density memories with low power dissipation is more desirable. Therefore, it is very useful to find a topology which serves both type of applications. In this paper a new high-speed keeper topology for large signal arrays (LSA) has been proposed which significantly improves read performance and is a high density design capable of supporting a larger number of bits per local bit line.

Besides the conventional keeper the delayed keeper technique is quite popular and there are several other reported techniques [3–16] to improve read performance. However, each of these techniques have some disadvantage either in density or power consumption of the circuit. The reported techniques are studied and discussed in detail in Section 2.

Register file (RF) compiler design prefers keepers that do not require fine tuning the keeper delay across the range of the LBL lengths that the compiler supports. The known keeper techniques [3–16] require separate delay settings tuned to different LBL lengths to balance V_{min} and performance for both Read-0 and Read-1 cases. Hence, for compiler design each LBL length has to have a custom keeper circuit or added selecting circuit is needed to select between ranges of keeper delay settings. The existing techniques therefore, add complexity or area or both to complier designs.

Usage of compiler generated memory instances have increased significantly in SoC design. ROM/RF memories are not exempt. In addition, the RF usage in SoCs are increasing rapidly [17–20]. It would be valuable to have a keeper technique that does not require fine tuning. Also, any test cost that is saved by not having to do die-by-die tuning may be significant. Separately the contention free nature of the keeper allows design optimization that leads to overall better V_{min}, power, performance and area.

This paper proposes this new keeper technique which combines both delayed and conditional delayed keeper concept to produce at par or better performance. The control circuit for the keeper transistor requires only an inverter and three additional transistors adding up to a total of five transistors. This topology does not require a series of delay chain buffers or complex delay tuning circuit. Only one inverter is capable of achieving the desired goal. Simulations in 14 nm process show that this technique is able to achieve matched or better V_{min} and performance while providing significant advantages in area and power over existing techniques for LBLs in the 8 to 64bit range.

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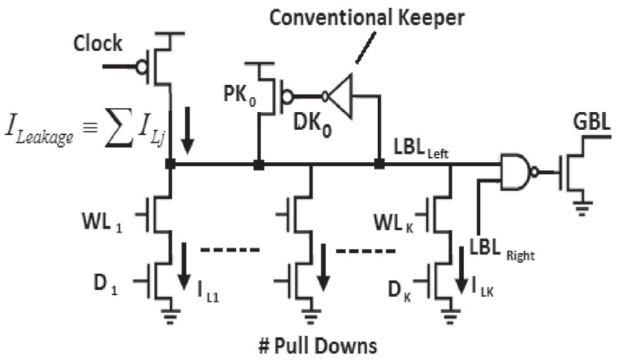

Fig. 1. Conventional keeper (CNVK) Topology [4].

The rest of the paper is organized as follows. The existing keeper techniques are discussed in section 2. At the end of this section we also provide a brief overview of the proposed new technique. Section 3 describes the proposed contention free delayed keeper design and the design considerations. Simulations are performed to compare the performance and functionality of the proposed technique with existing topologies in section 4. Section 5 concludes the paper.

2. Background and related work

A conventional local (large signal) sensing topology [4–6] in the read path of a register file is shown in Fig. 1. The contention between the PMOS keeper strength and NMOS pull-down stack in the register file bit-cell limits read V_{min} (minimum voltage of operation). Better V_{min} may be achieved by weakening the keeper (PK_0) which can be obtained by weakening the PMOS. Weaker keeper helps to lower V_{min} up to a certain point and after that further lowering is not possible because of the leakage ($I_{Leakage}$) noise limit. Leakage increases DC voltage drop in the local bit line, thereby, raising the possibility to a failed read zero (READ-0).

A possible solution is to use a clock-delayed keeper (CDK) [1,8] (shown in Fig. 2) which can reduce read V_{min} further by reducing contention between keeper PMOS stack and pull down NMOS stack during the initial part of the evaluation. Fig. 3 shows the delayed keeper functional modes. In this technique, at the beginning of the evaluation period the keeper is deactivated using a delay element for a certain period of time which helps to remove the contention and make the read evaluation move faster. Control signal (DK_0) for this keeper is produced by the pre-charge clock propagating through the delay elements. In Fig. 3 the initial delay required for end of pre-charge (EOP) margin is TD_1 and TD_2 delay added to create the desired contention free time. Hence, the overall required delay will be TD = TD_1 + TD_2. Generally the time required by LBL to complete discharge without keeper is also essential to eliminate contention. That's why when the number of pull downs increases, more delay elements are required since LBL takes more time to discharge.

Large number of delay elements signifies less time for keeper to turn on for READ-0 which potentially is not favorable for READ-0. To overcome this issue, next possible option is to use a Conditional Keeper (CNDK) [1,4–7,9,16] which is shown in Fig. 4. In this technique, at the beginning of the evaluation period, only a small fraction of the keeper (PK_0) is activated, to balance the READ-0 and READ-1 performance. After certain time interval, governed by a delay element, a strong keeper (PK_1) is activated conditionally by monitoring the LBL node. In this topology, generally without keeper the time required by LBL to reach 50% of V_{CC} is the sufficient delay to eliminate contention as PK_1 control signal (DK_0) is directly gated with LBL. This indicates that CNDK needs comparatively less number of delay elements compared to CDK and thus accounting for better area.

Though both of the above techniques improve performance but they suffer from the following drawbacks:

a. The duration of the contention free time is difficult to predict. For different number of pull downs per local bit line (LBL) the time may vary. Large number of pull downs mean higher LBL load and hence, the need for longer delay and more delay elements. If the same sensing design is required to support a large range of bits per bit line across different process, voltage and temperature (PVT) skew corners then different sets of programmable delay elements [10] are required to produce the necessary delay thereby, increasing design complexity.
b. For bit lines with large number of bits more delay is required resulting in longer buffer delay chains and increased area.
c. Designs with larger number of bits per LBL require finer granularity in keeper delay control to balance between successful READ-1 and successful READ-0. It may be noted that READ-1 fails happen when there is not enough contention free time during evaluation and READ-0 fails happen due to the leakage noise floor.

Due to the above reasons the techniques discussed require either custom keeper design for each LBL length or a significant area overhead needs to be paid by all granularities of LBL length. Both are not desirable

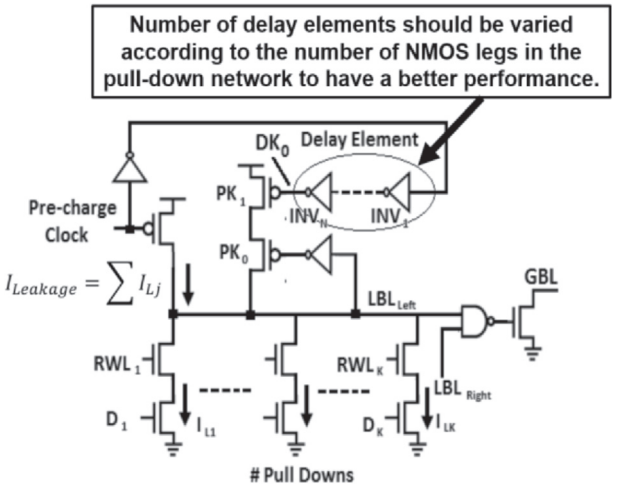

Fig. 2. Clock delayed keeper (CDK) topology [8].

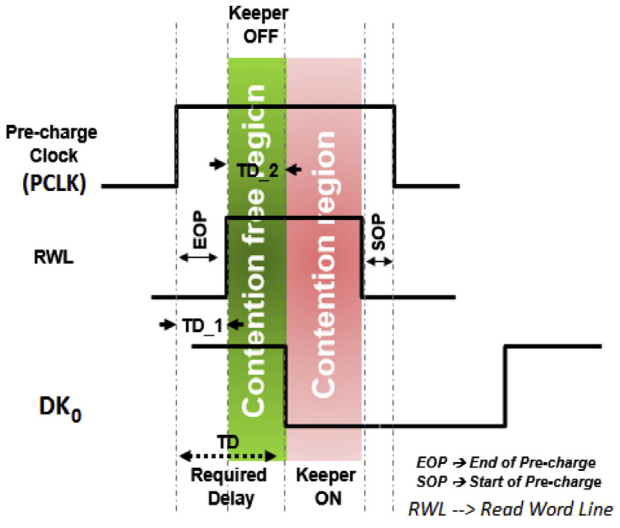

Fig. 3. CDK functional waveforms.