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MOSCAP compensation of three-stage operational amplifiers: Sensitivity and robustness, modeling and analysis

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ABSTRACT

Using MOSCAPs for compensation can reduce the area needed for their implementation. However; these capacitors are highly nonlinear and their value changes when the voltage across their terminals is changed. Different compensation topologies do not exhibit equal sensitivity to the time-dependent variation of MOSCAP compensation capacitors. Therefore; the selection of a proper compensation technique is considered as an important step before its implementation. In this paper, the goal is to study the existing compensation techniques and their behavior in the presence of compensation capacitor uncertainty and MOSCAP nonlinearity. For such regard, opamps are first designed for equal performance metrics such as: gain bandwidth product, phase margin and settling time. Then the sensitivities of the different structures are evaluated. Ultimately, the least sensitive structures can be chosen as the best choice for implementation. Based on the knowledge of the authors, no such thorough analysis has been ever performed before. A state-space model is suggested to analyze different compensation topologies and to calculate the harmonic distortions and find the most robust structures. These results are compared with circuit level results. It is shown that the CFCC compensation method can lead to creation of least harmonic distortion.

1. Introduction

Opamps are widely used in many analog-digital systems [1]. In today's integrated circuits, it is preferable to combine the analog and digital circuits on a single chip to minimize the size and enhance the performance. This means that all analog circuit components should be realized using the technology which is optimized for digital circuits. Components such as capacitors, inductors and resistors can be quite area consuming in this case and they usually take up the most space in analog circuits. When designing opamps, compensation capacitors usually take up the most space. A practical way to reduce their sizes is to use the Gate-Bulk capacitors of MOS transistors (MOSCAPs) instead of the conventional metal-insulator-metal (MIM) capacitors. Thay have a high capacitance density but they are highly nonlinear. The mentioned nonlinearity results in the creation of harmonics. For some applications these harmonics can be harmful and for some applications the existance of harmonics can be neglected. The goal of this paper is to analyze, model and investigate which compensation technique has a lower harmonic distortion and which one is the most robust against the variation of compensation capacitors.

Based on the type of compensation network, three-stage opamps can be divided into different categories. The main conventional method used in these structures are feedforward and feedback paths that are active or passive, such as: Miller compensation techniques [2–8], nested Miller compensation using nulling resistor [9,10], nested Miller compensation with current buffer [11,12], reverse nested Miller compensation technique [13], compensation with active forward path [14,15], nested Miller compensation with nested transconductance stage [12,14,16–22], damping-factor-control frequency compensation technique [[23–25]], compensation with impedance adapting [26], frequency compensation technique by single Miller capacitor [27]. To obtain the optimal frequency characteristics for low-voltage operational amplifier design, some techniques have been proposed in Refs. [1–4,28,29]. Moreover; some other design methods have been proposed to achieve optimal settling time in switched-capacitor and analog-to-digital converters [1,30–36].

In this paper, the compensation capacitors are going to be replaced with MOSCAPs and the goal is to compare different three-stage compensation topologies to find the most robust topology. For this purpose, parameters such as GBW, PM, settling time and slew rate are taken into account. A MOSCAP's value changes when the voltage across its terminal changes. The terminal which is connected to the opamp's output changes the most. The other terminal's voltage also changes, but not as

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much. First of all MOSCAPs are modelled as ordinary capacitors which can have a maximum ±50% variation based on the voltage across their terminals. The open-loop transfer functions of different compensation topologies are extracted from the literature. We design the opamps for a 100 pF load, 10 MHz bandwidth, 100 dB DC gain and a 60° PM and investigate the effect of compensation capacitor variation on parameters such as GBW, PM and settling time.

Apart from affecting PM, GBW etc., MOSCAPs can cause harmonic distortion. Therefore, different topologies should also be compared based on their harmonic magnitudes. The state-space (SS) equivalent model for the transfer function of opamps along with a voltage dependent capacitor model is used to calculate the harmonics in a system-level method. Analyzing the opamps designed for equal GBW, PM and equal load capacitance reveals that there can be a 12 dB gap between the third harmonic magnitudes obtained for different compensation topologies. Therefore choosing the right compensation topology can be very important harmonic-wise.

The rest of this paper is organized as follows: In Section 2, the gate-bulk capacitors, series compensated depletion-mode (SCDM) MOSCAPs, and parallel compensated depletion-mode (PCDM) MOSCAPs, are investigated. A brief design procedure (for three-stage operational amplifiers) for each compensation technique is presented in Section3. The sensitivity of different compensation techniques to the uncertainty of compensation capacitors is investigated in Section 4 and the most robust structures are introduced. In Section 5 the proposed system-level state-space model for obtaining the harmonics is explained and the topologies which produce the highest and lowest magnitudes of harmonic distortions are introduced. Section 6 compares the circuit level harmonics with the proposed state-space model and the final section is devoted to conclusions. All the simulations that are performed in Sections 4 and 5 are system level. To verify these results transistor level simulations are performed in Section 6.

2. Gate-bulk capacitor of a MOSFET

Metal-insulator-metal (MIM) capacitors are used for most analog integrated circuit applications; however, they cannot be integrated in every technology as they need additional process masks. Moreover, these components occupy a large silicon area. For a large category of applications MOS capacitors (MOSCAPs) can be considered as an affordable alternative for the capacitors required by analog circuits [37–41]. In contrast with MIMs, it will be shown that MOSCAPs are highly nonlinear. In order to employ the gate-bulk capacitance of a MOS transistor, the transistor's gate is considered as one of capacitor terminals and its drain, source and bulk are connected together to create the other one. As seen in Fig. 1(a), this structure is hereafter referred to as a “simple MOSCAP”. Fig. 2(a) shows the gate-bulk capacitance variation of a MOS device simulated in a 0.18-μm CMOS technology. Although simple MOSCAPs are advantageous in terms of occupying area, but they need high bias voltages to become relatively linear, hence they are not suitable for many low-voltage applications. Parallel and serial combination of simple MOSCAPS can be used to improve linearity. These structures use the depletion region of the transistor to provide better linearity. The series compensated depletion-mode (SCDM) MOSCAPs and parallel compensated depletion-mode (PCDM) MOSCAPs are depicted in Fig. 1(b) and (c).

In a series compensation technique [39], two MOS capacitors are connected anti-serially. Fig. 1(b) shows this configuration for two p-channel MOS capacitors. The desired capacitance is available between nodes A and B. To have a low parasitic capacitance at the floating node (C), the gates of M1 and M2 are connected together. Also, an additional transistor (M_3) is used which is biased in the sub-threshold region and acts as a high resistance element to prevent the floating node from charging. The area of M_3 should be small compared to M_1 and M_2 to avoid a significant parasitic capacitance at node C. The C-V plot of a SCDM-MOSCAP operating under an asymmetric condition is shown in

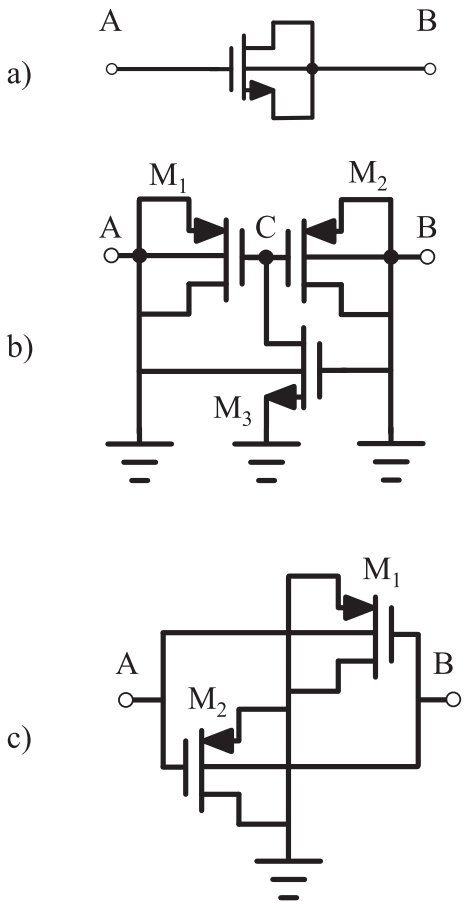

Fig. 1. MOSCAP topologies (a) Simple MOSCAP (b) SCDM (C) PCDM.

Fig. 2 (b). A 0.18 μm standard digital CMOS technology with $t_{ox} = 4.08$ nm is used for all the simulations in this paper. The threshold voltage for nMOS transistors is $V_{Tn} = 0.5$ V and for pMOS transistors is $V_{Tp} = -0.51$ V. For M_1 and M_2, we used W_1=W_2=10 μm and $L_1 = L_2 = 10$ μm. To be able to compare MOSCAP structures together, the normalized variation is defined according to (1):

$$Normalized\ variation = \left(\frac{C_{max} - C_{min}}{C_{max}}\right) \times 100 \quad (1)$$

Fig. 2(b) shows the C-V plot of a SCDM-MOSCAP for the bias voltage range of zero to 1 V. The normalized variation is now about 19.55%. The capacitance per unit area for this MOSCAP is about 0.67 fF/μm^2 for $V_{AB} = 0$ V and 0.54 fF/μm^2 for $V_{AB} = 1$ V. In a parallel compensation technique [40], two MOS capacitors are connected in an anti-parallel form. Fig. 1(c) shows this configuration for two p-channel MOS capacitors. The C-V plot of a PCDM-MOSCAP operating under an asymmetric condition ($V_{AB} = 0$ V–1 V) is shown in Fig. 2(c). Here the variation is about 45%. It is seen that the nonlinearity has increased severely. This amount of nonlinearity is unacceptable for many applications. The capacitance per unit area for the asymmetrically operated MOSCAP is approximately 4.17 fF/μm^2.

In Table 1 the different MOSCAP topologies are compared. From the results presented in Table 1and regardless of the process, SCDM has better linearity compared to other MOSCAPs at the cost of significantly more area and complications related to gate charging. Uncompensated pMOS, on the other hand, is the simplest and occupies the least area at the cost of worst nonlinearity. With exception of SCDM, it is also clear that all MOSCAPs occupy less area compared to MIMs. Since PCDMs do not have any design complications and they are much smaller than SCDMs, unless otherwise stated, these components are utilized in the